

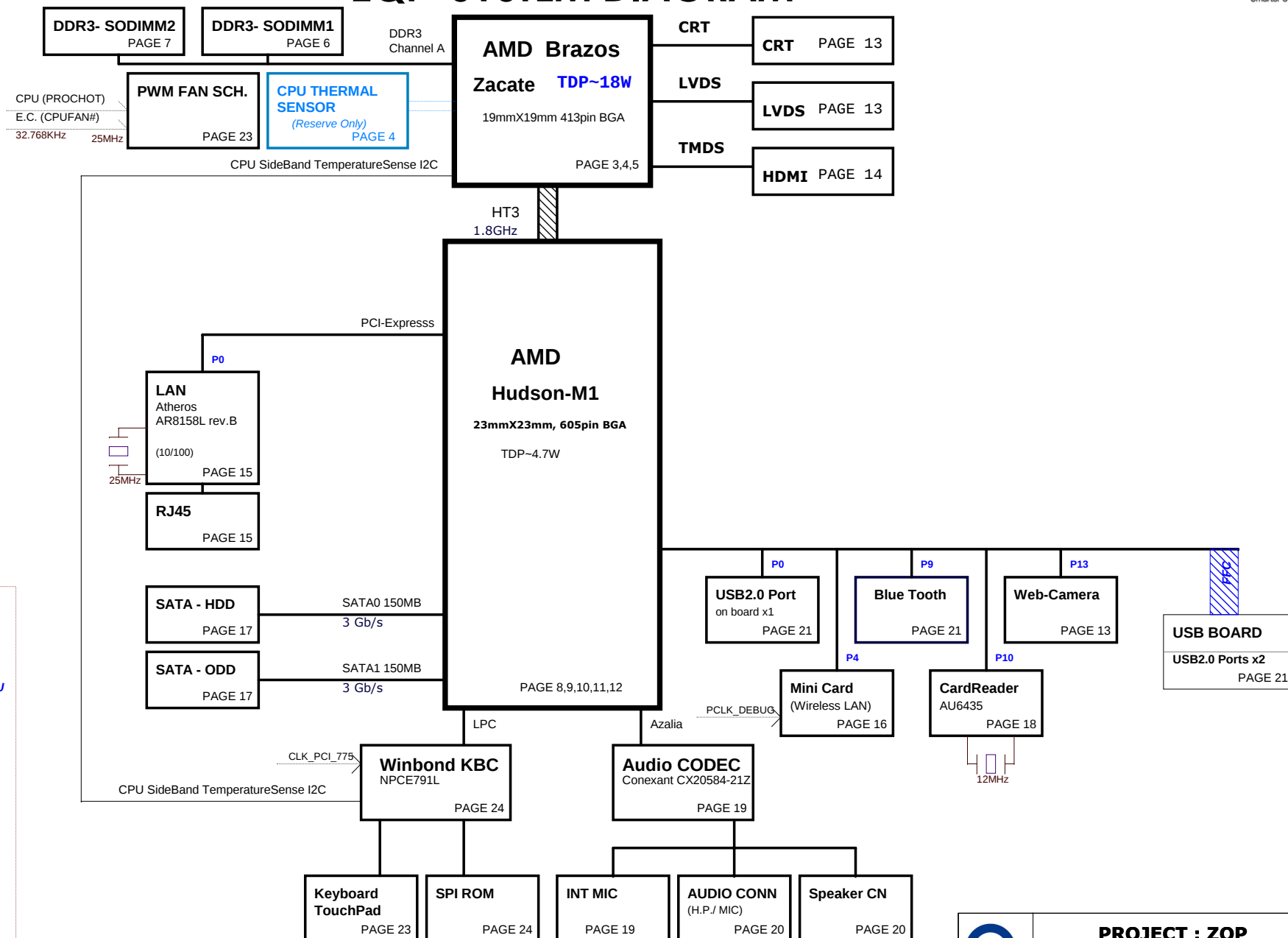
ZQP SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

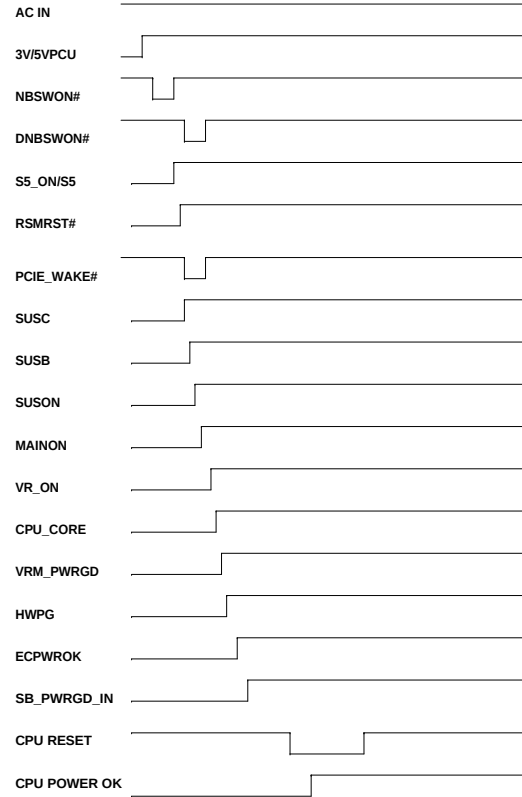
HDMI@ ----> HDMI option
SP@ ----> Board ID/Strap pin
H@ ----> 家電下鄉

UMA **REV: B**



PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	ONTARIO MEM & PCIE I/F(1/3)	
4	ONTATIO DISPLAY/CLK/MI(2/3)	
5	ONTARIO POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM (STD=8)	
7	DDR3 SO-DIMM (STD=4)	
8	HUDSON PCIE/LPC/CPU I/F(1/5)	
9	HUDSON ACPI/GPIO/USB(2/5)	
10	HUDSON SATA/BIDS(3/5)	
11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	CRT/LVDS/CCD	
14	HDMI	
15	LAN AR8152	
16	MINI PCI-E	
17	HDD /ODD	
18	CARD READER	
19	AUDIO - CONEXANT 20584	
20	AUDIO JACK CONN	
21	USB / BT /TP	
22	LED / NUT	
23	KB/FAN/TP	
24	WPCE791 /FLASH	
25	CHARGER (ISL88731A)	
26	SYSTEM 5V/3V (RT8223M)	
27	CPU CORE (OZ8380)	
28	VCCP 1.1V (G5602)	
29	+1V(G5602)	
30	DDR 1.5V (RT8207A)	
31	+1.8V/Discharge/Thermal Protection	
32	Change list	

Power Sequence



Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

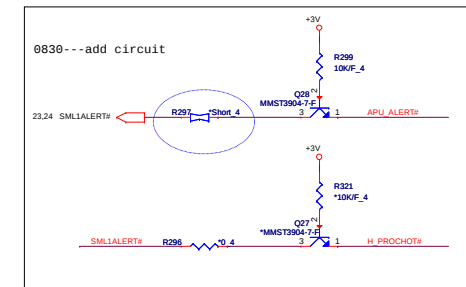
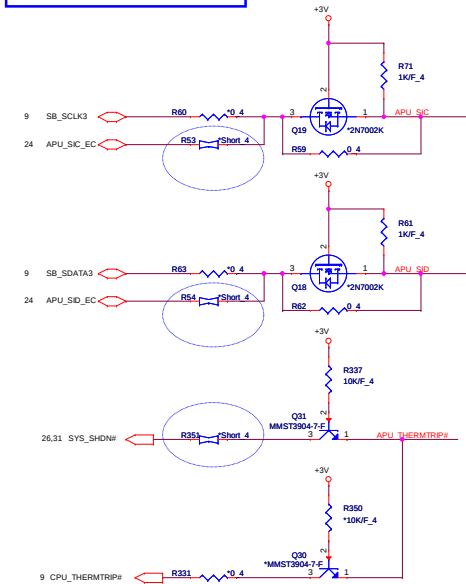
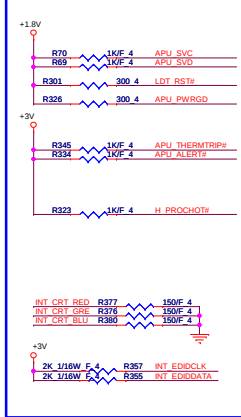
KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

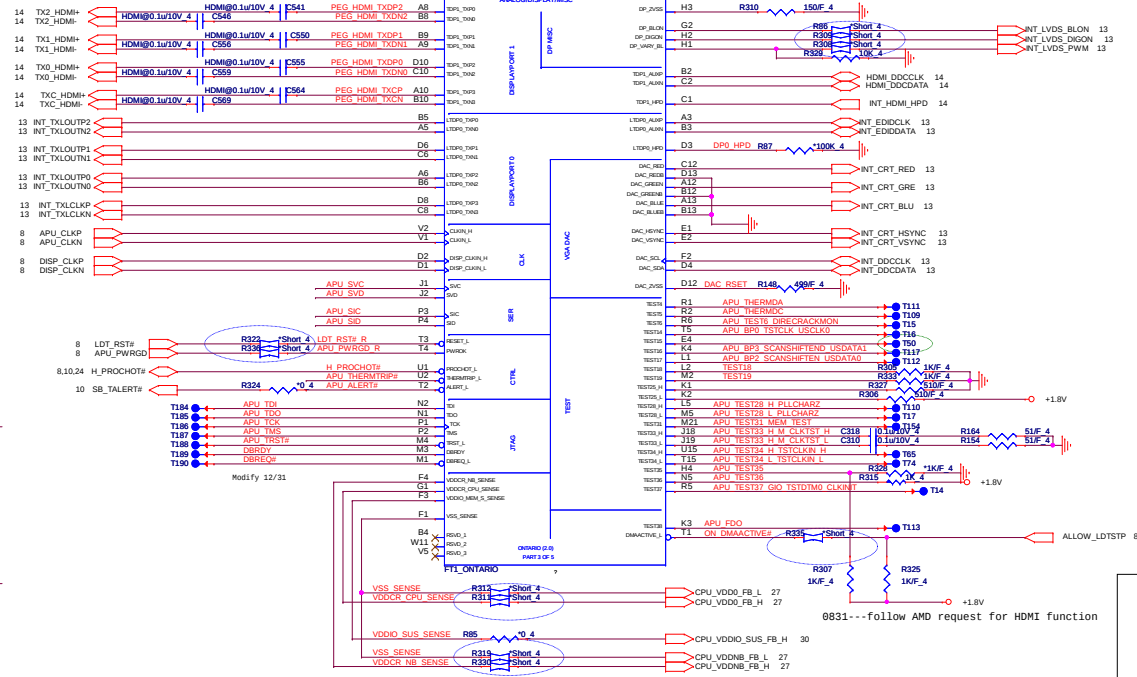


E350	AJ0E350VT01
C50	AJ00C50VT02

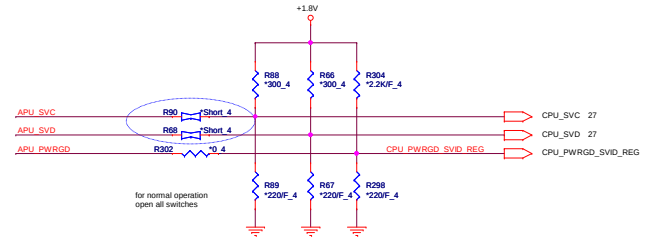
+1.8V 5.31
+3V 5.6,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31

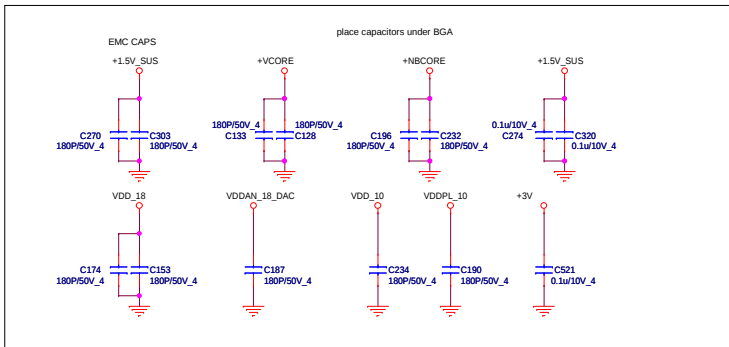
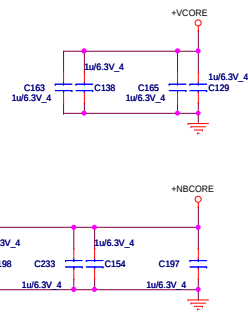


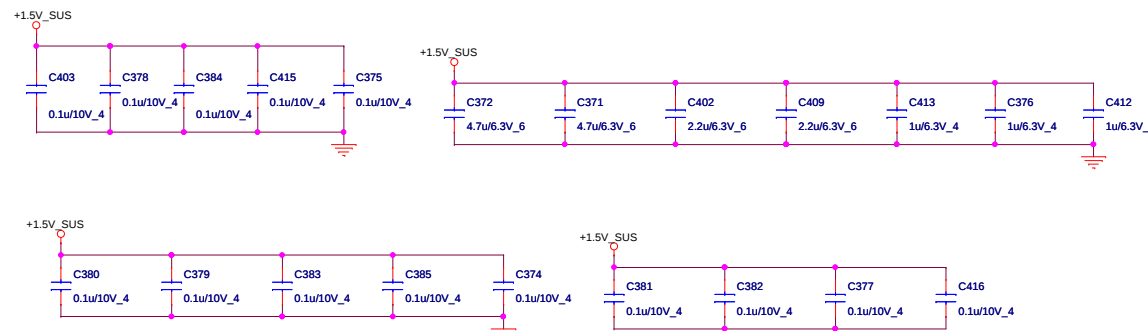
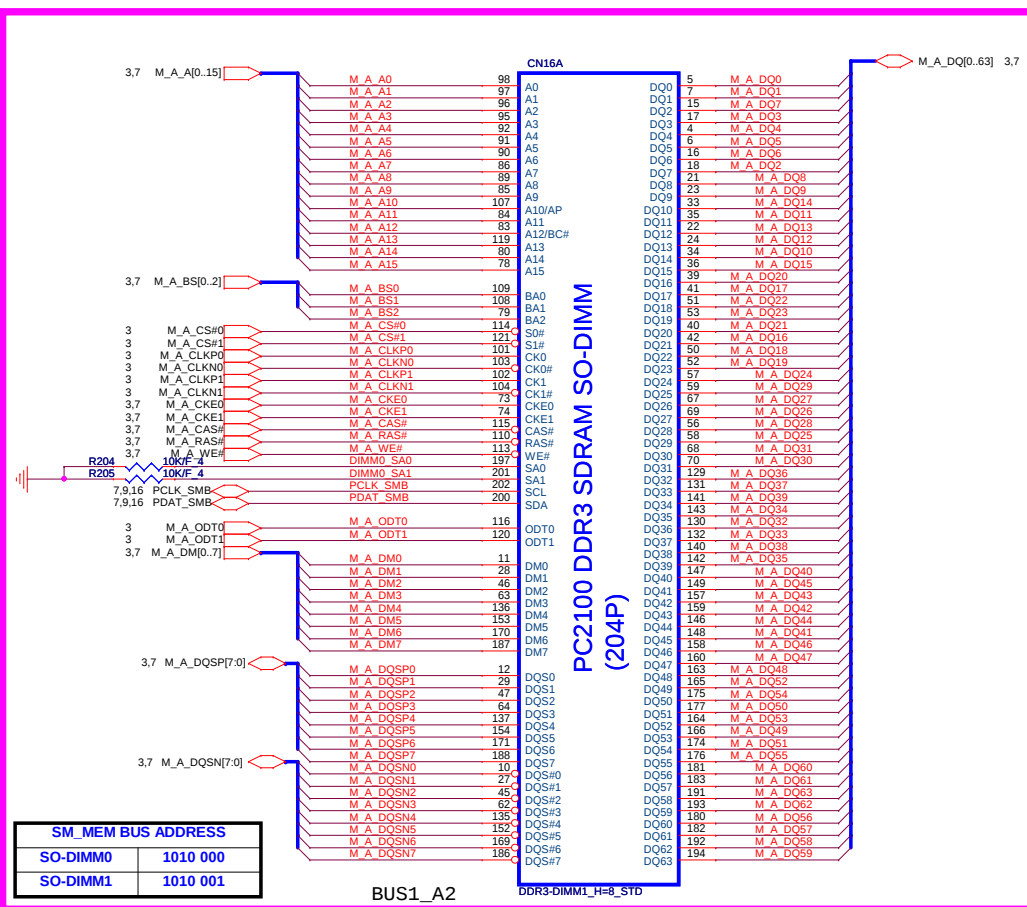
AGS HDMI 01/18



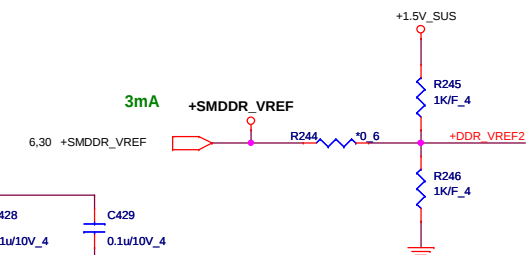
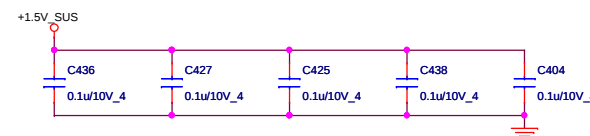
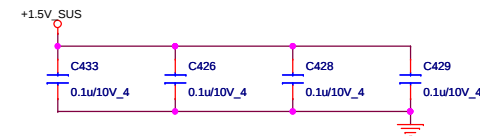
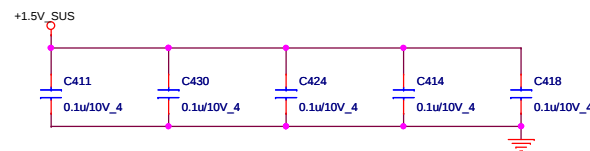
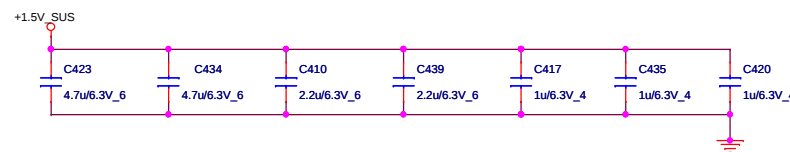
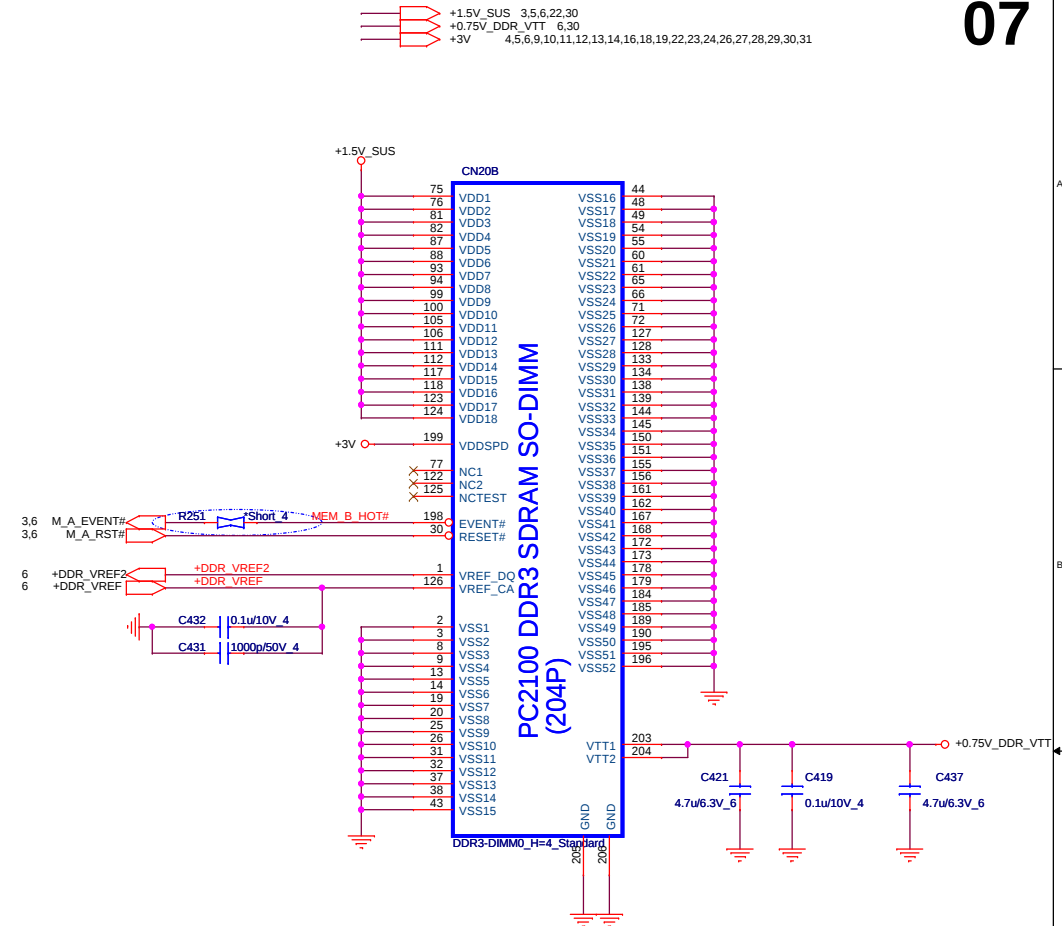
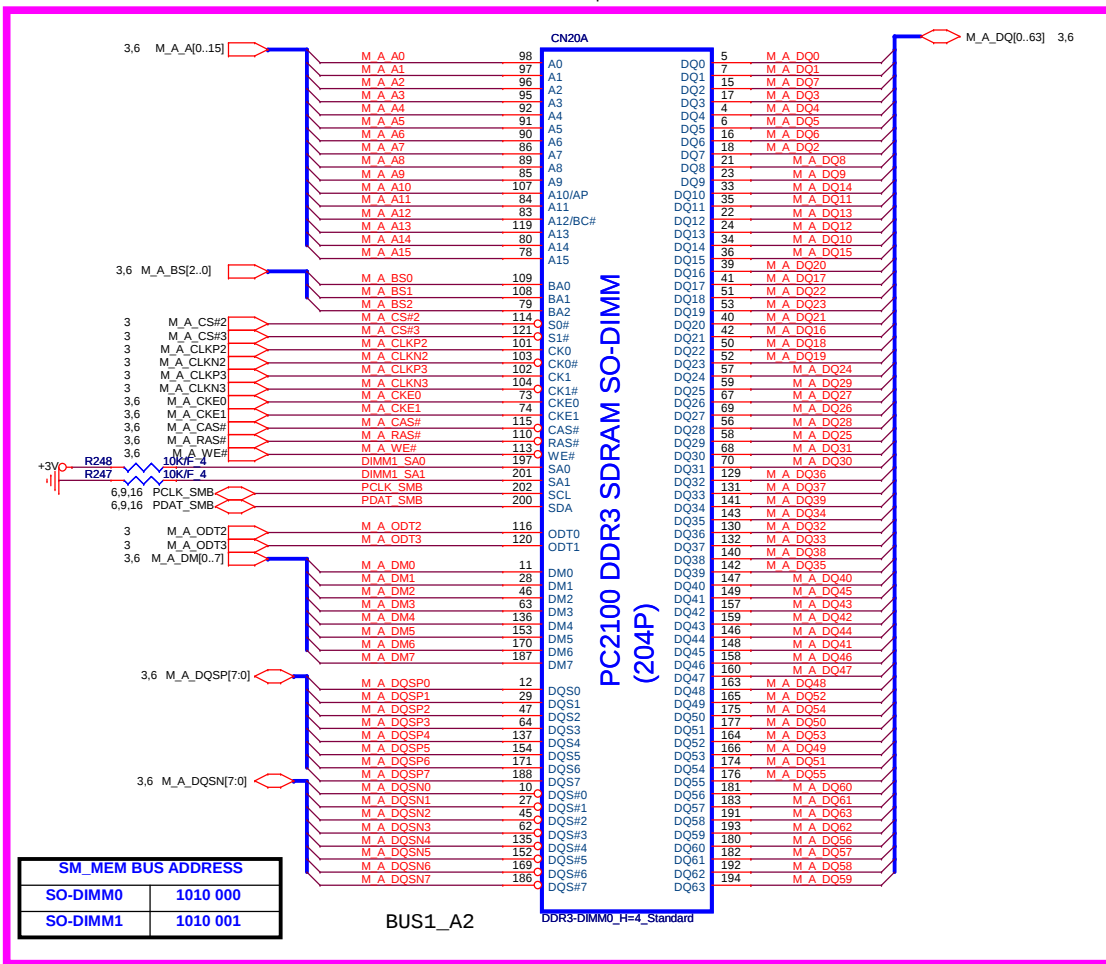
VID Override Circuit





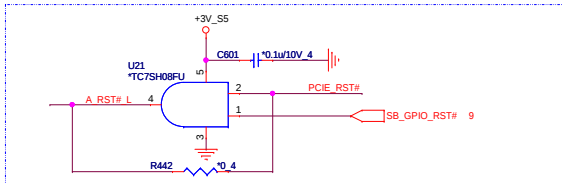
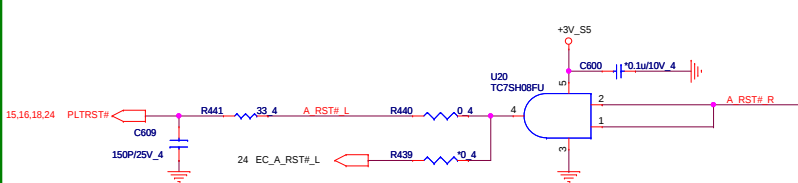


www.vinafix.vn



PROJECT : ZQP
Quanta Computer Inc.

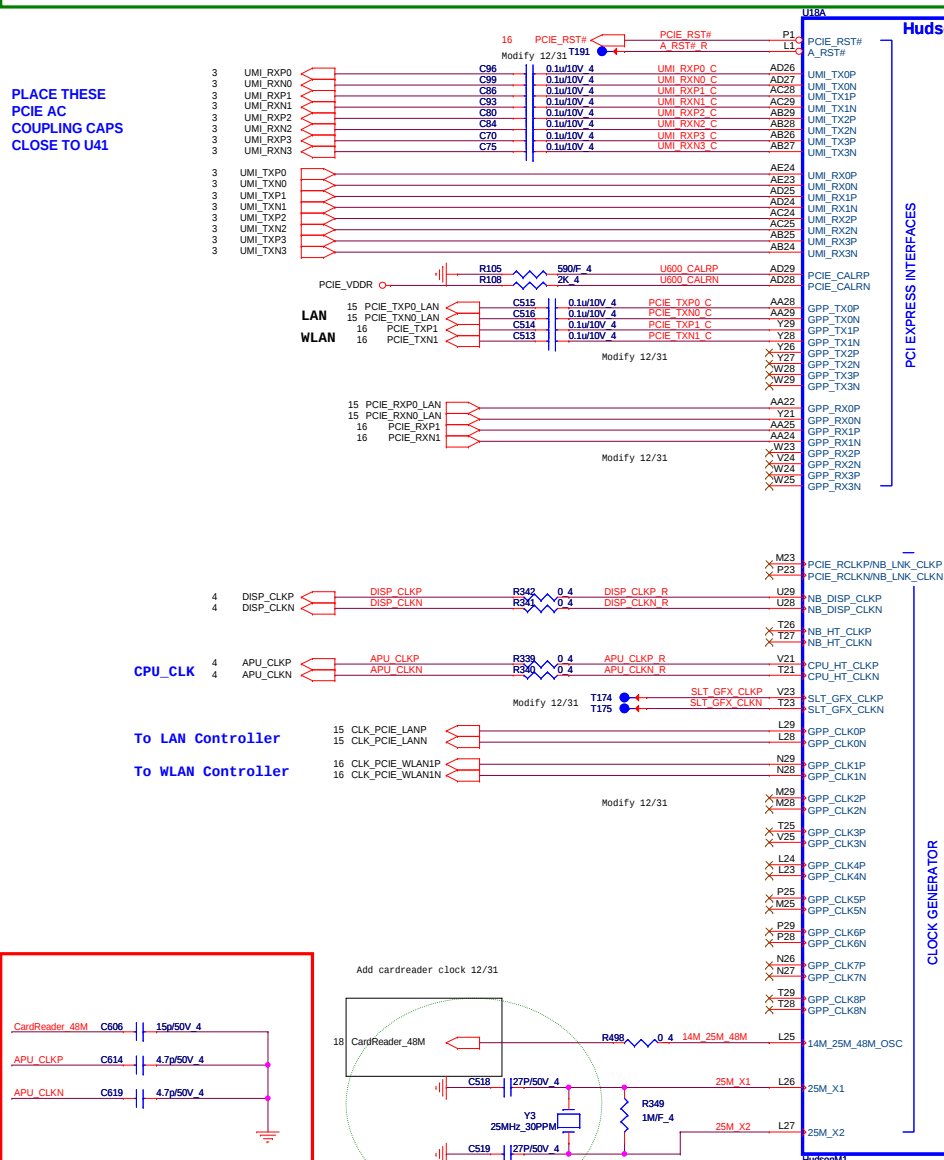
Size	Document Number	Rev
	DDR3 SO-DIMM (STD)	1A
Date:	Tuesday, March 15, 2011	Sheet 7 of 32



PCIE_VDD# 11
+3V_S5 9,10,11,12,15,21,22,26
+3VPCU 13,22,23,24,25,26,31
+5VPCU 26,27,28,31

This page is different AMD Nil expect RTC circuit

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U41



BG625000486

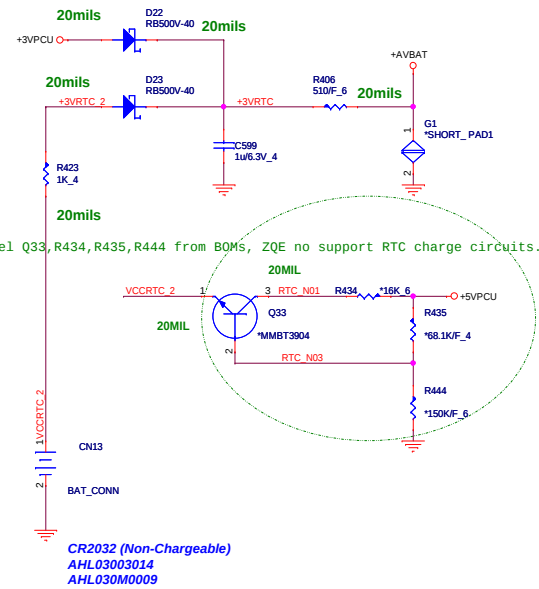
Hudson M1 Part 1 of 5

STRAP Function
To EC

Debug STRAPs

All the PCI bus has
build-in Pull-Up/Down
resistors

RTC



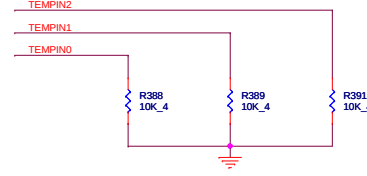
CR2032 (Non-Chargeable)
AHL03003014
AHL030M0009

To STRAPs Page

INTRUDER_ALERT# Left not connected (Southbridge
has 50-kohm internal pull-up to VBAT).



AMD recommend : TEMPIN0 / TEMPIN1 / TEMPIN2
can not maintain on floating stages when without usage.
Do not care pull high or pull down.

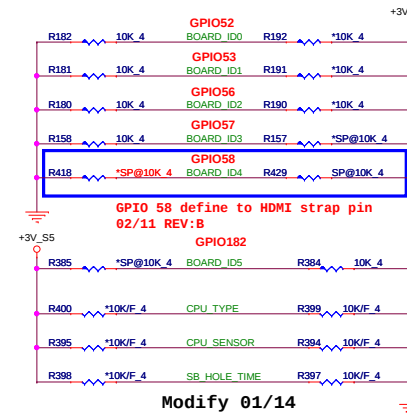


0831--modify location

MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0
SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0
DUI1/MK2	GPIO56
MK2.0 AMD	1
DUI.0 AMD	0

	GPIO57
(Dis) SW	1
UMA	0
	GPIO58
With HDMI	1
Without HDMI	0
	GPIO182
PX4.0	1
PX3.0	0



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

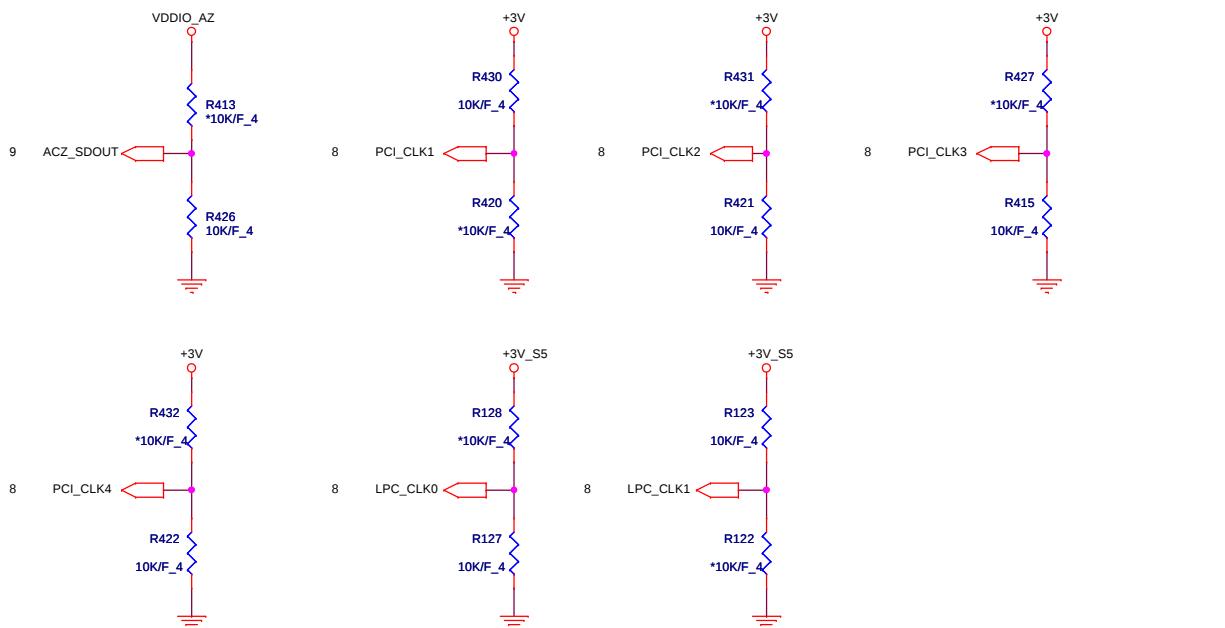




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K, confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

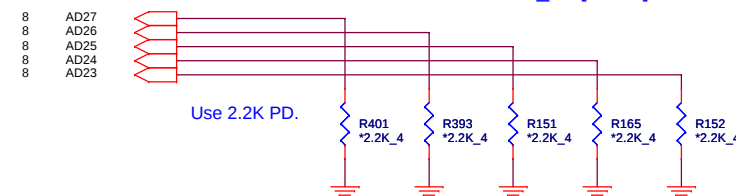
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,10,11,15,21,22,26

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



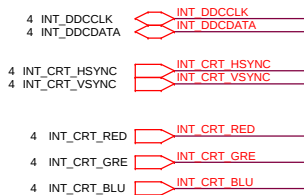
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



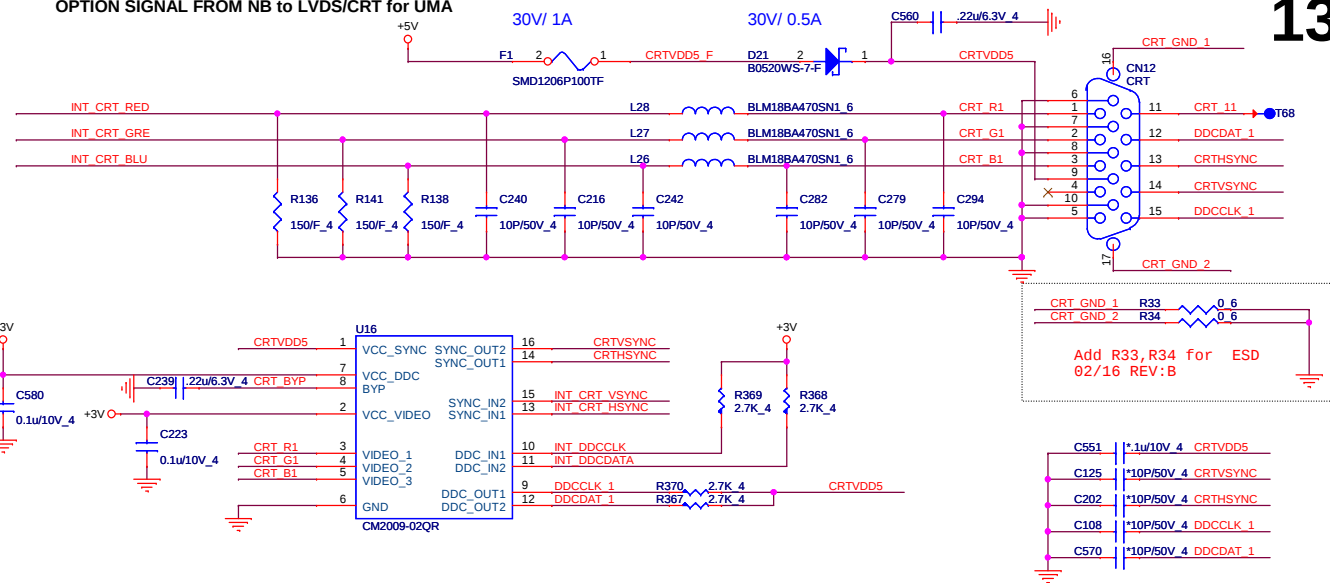
PROJECT : ZQP
Quanta Computer Inc.

Size Document Number
HUDSON STRAPS/PWRGD(5/5) Rev 1A
Date: Tuesday, March 15, 2011 Sheet 12 of 32

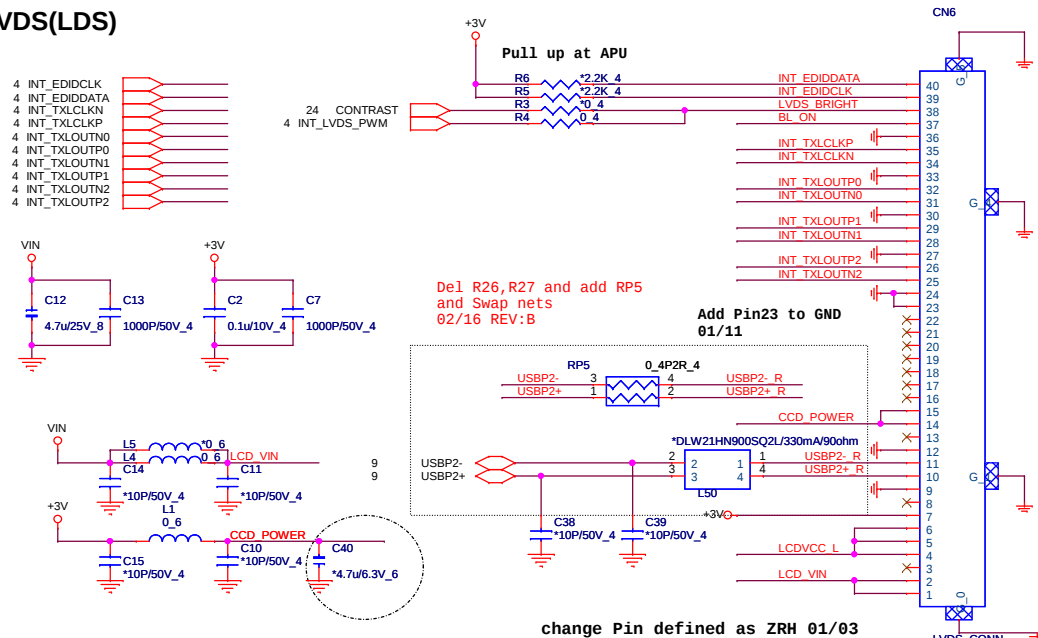
CRT



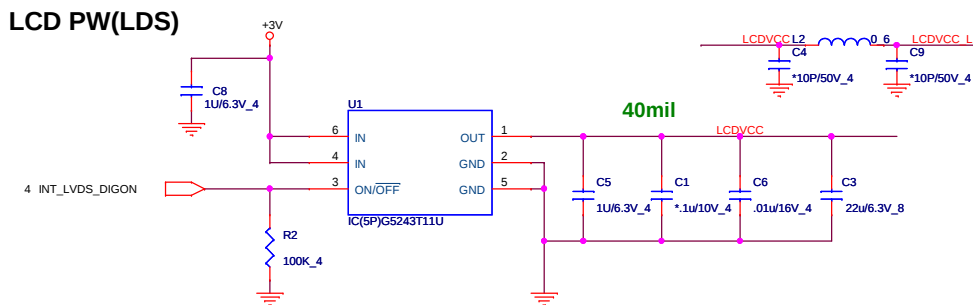
OPTION SIGNAL FROM NB to LVDS/CRT for UMA



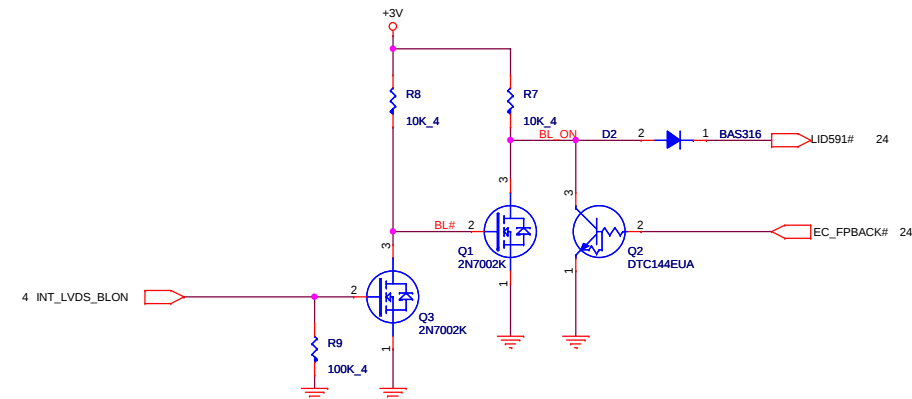
LVDS(LDS)



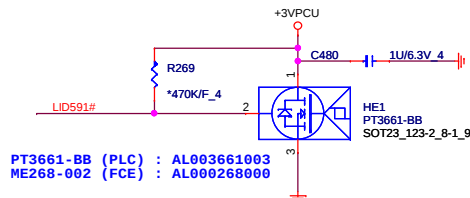
LCD PW(LDS)



Backlight Control(LDS)



Lid Switch (HSR)

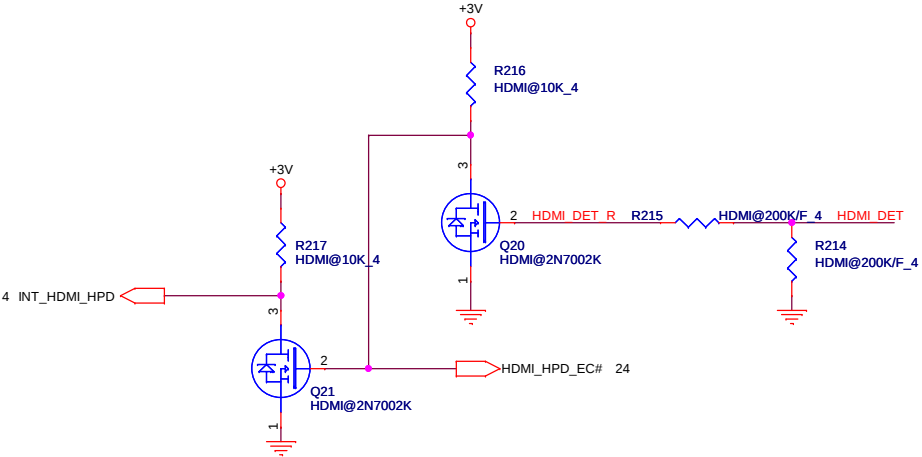


HDMI SDVO I2C Control



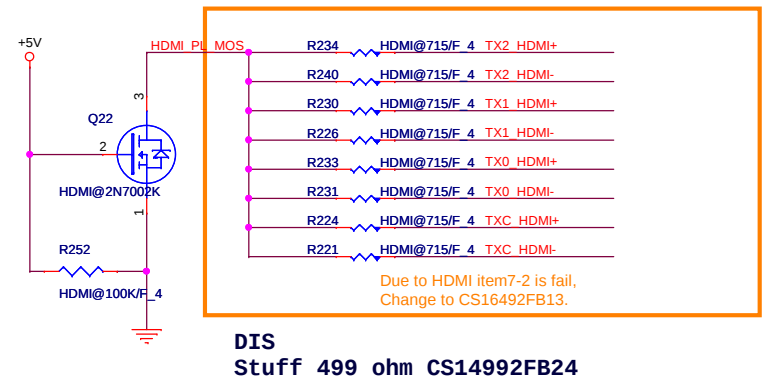
HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



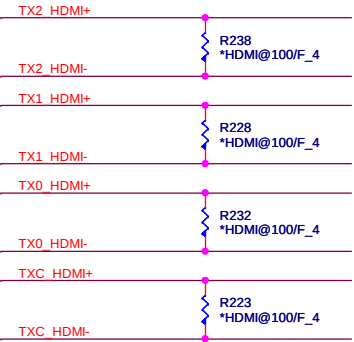
HDMI (HDM)

Close to HDMI Connector



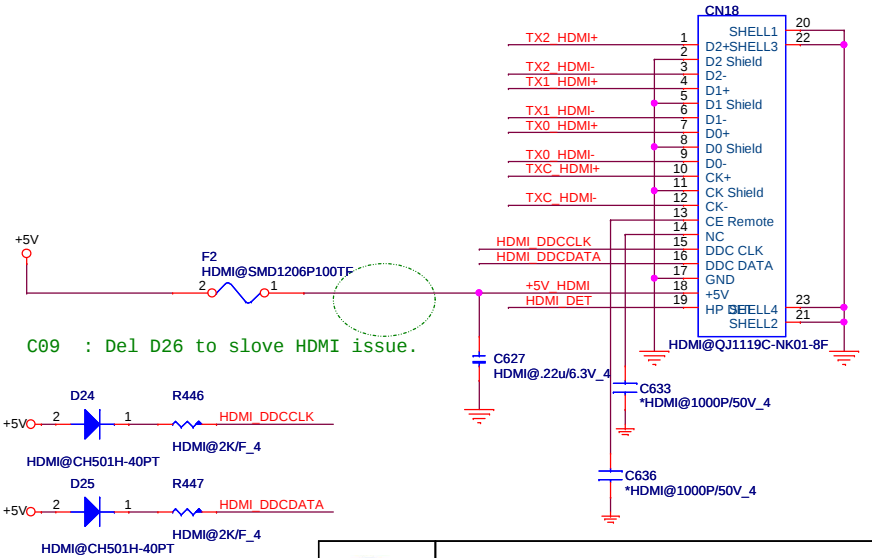
EMI reserve for HDMI(EMC)

Close connector



Added HDMI function
01/19 REV:B

HDMI PORT (HDM)



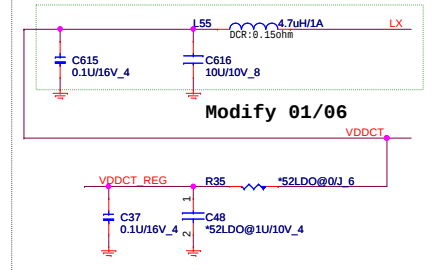
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
Date:	Tuesday, March 15, 2011	Sheet 14 of 32

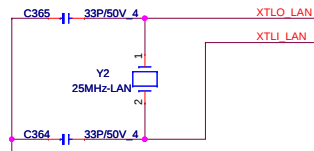
<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

<Layout note>
Close to Pin1

If use LDO mode L55 no stuff

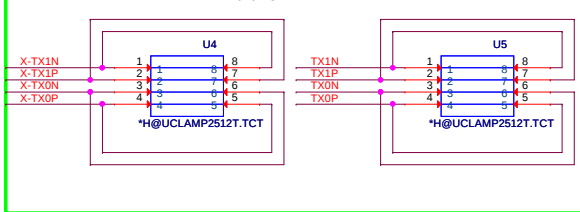


Modify 01/06

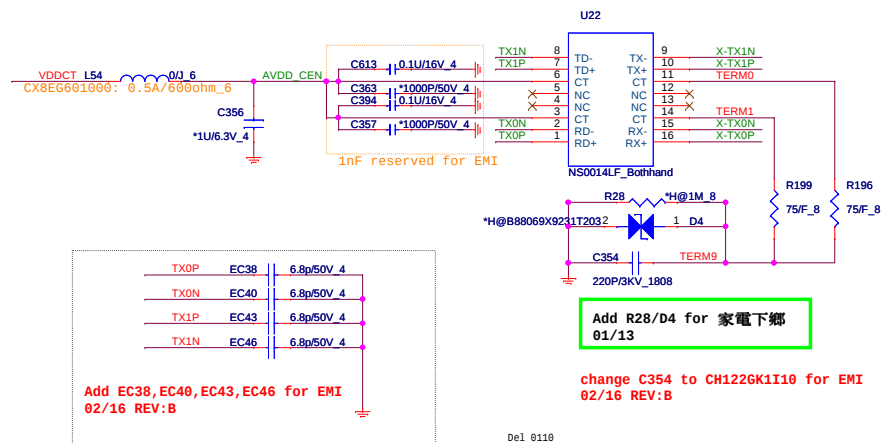


BG625000486

Add R28/D4 for 家電下鄉
01/13



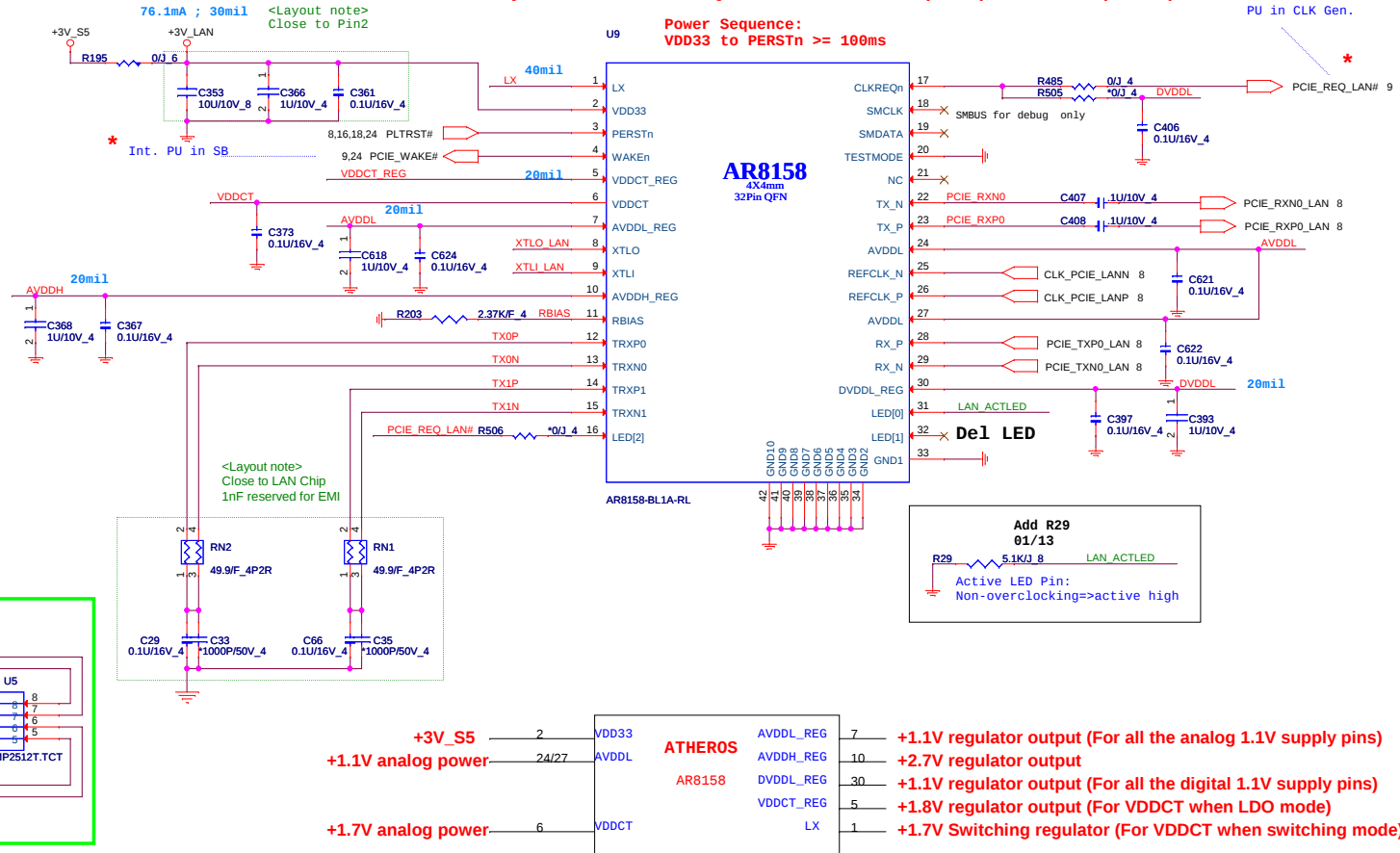
exchange pair 0/1
0110



Del 0110

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms



AR8158
4X4mm
32Pin QFN

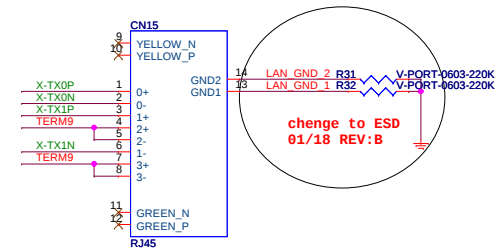
Add R29
01/13
R29 5.1K/0.8
LAN ACTLED
Active LED Pin:
Non-overclocking=>active high

+3V_S5	2	VDD33	7	+1.1V regulator output (For all the analog 1.1V supply pins)
+1.1V analog power	24/27	AVDDL	10	+2.7V regulator output
		AVDDH_REG	30	+1.1V regulator output (For all the digital 1.1V supply pins)
		DVDDL_REG	5	+1.8V regulator output (For VDDCT when LDO mode)
+1.7V analog power	6	VDDCT	1	+1.7V Switching regulator (For VDDCT when switching mode)

TRANSFORMER (LAN)

RJ45 Connector (LAN)

Del LAN LED 01/05



change RJ45 connector without LED
03/02

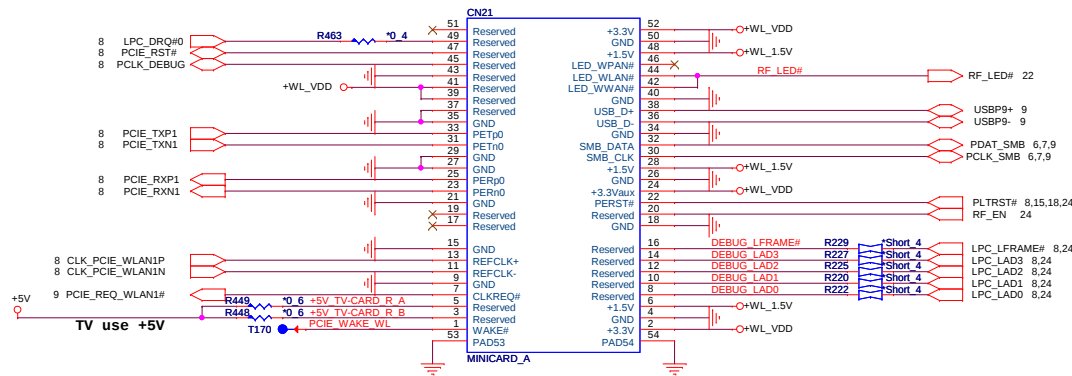
We will change RJ45 connector

PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number	Rev
	LAN AR8158L	1A
Date:	Tuesday, March 15, 2011	Sheet 15 of 32

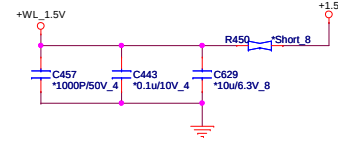
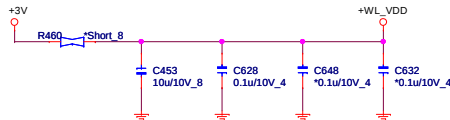
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Debug



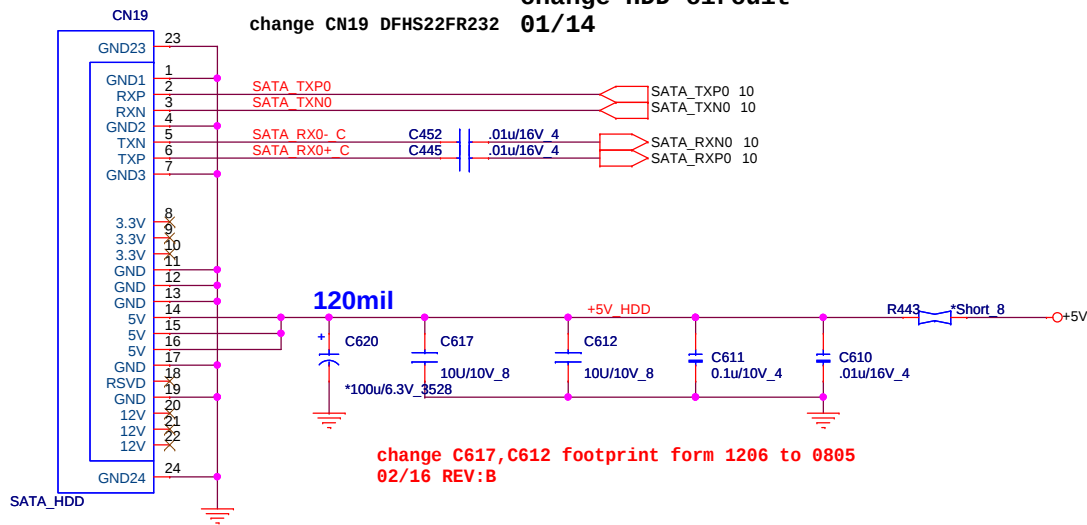
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E card	1A
Date:	Tuesday, March 15, 2011	Sheet 16 of 32

SATA HDD

change HDD circuit

change CN19 DFHS22FR232 01/14

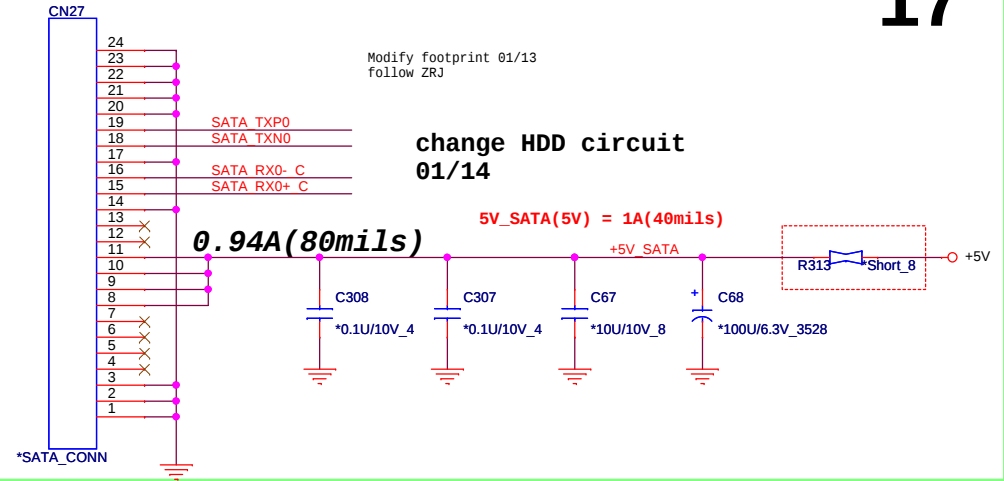


SATA HDD(HDD)

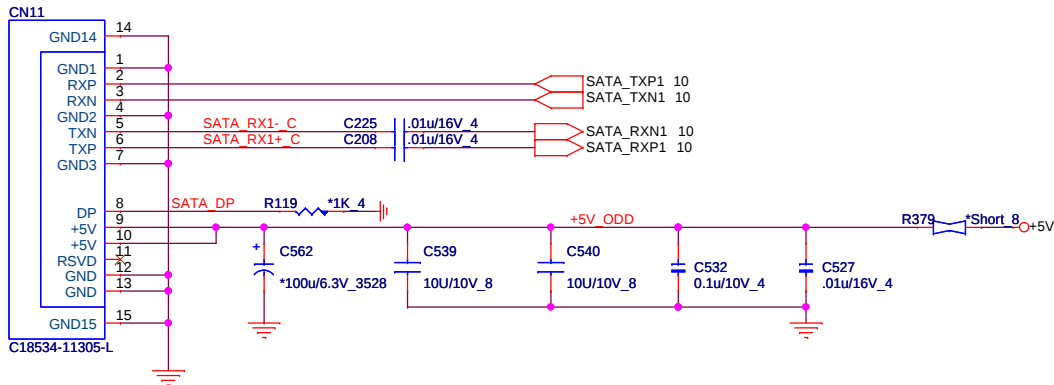
17

Modify footprint 01/13
follow ZRJ

change HDD circuit
01/14



SATA ODD



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

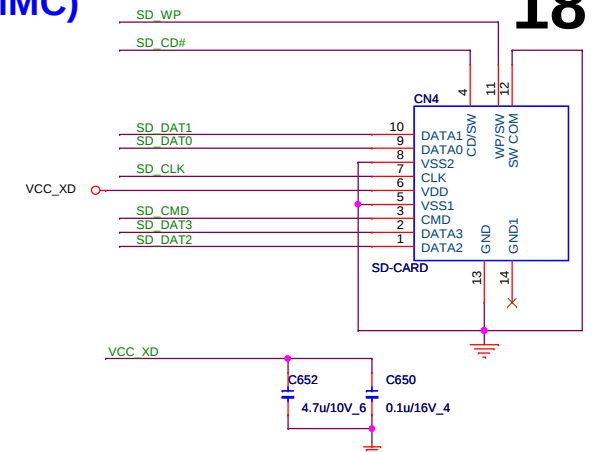
Date: Tuesday, March 15, 2011 Sheet 17 of 32

CARD READER Controller AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

Main	DFHS11FR011
Second	DFHS11FR033

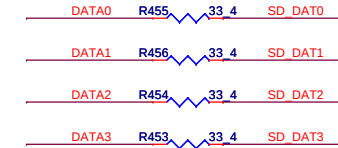
18



Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

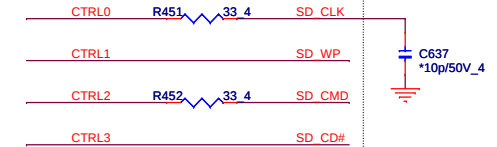
CTRL0, CTRL 1 trace length shorter ,
and surround with GND.

The trace length difference for each card interfaces should be
smaller than 500 mil



Close to connector

CLK length should be as short as possible. Shorter than
1200 mil is good.

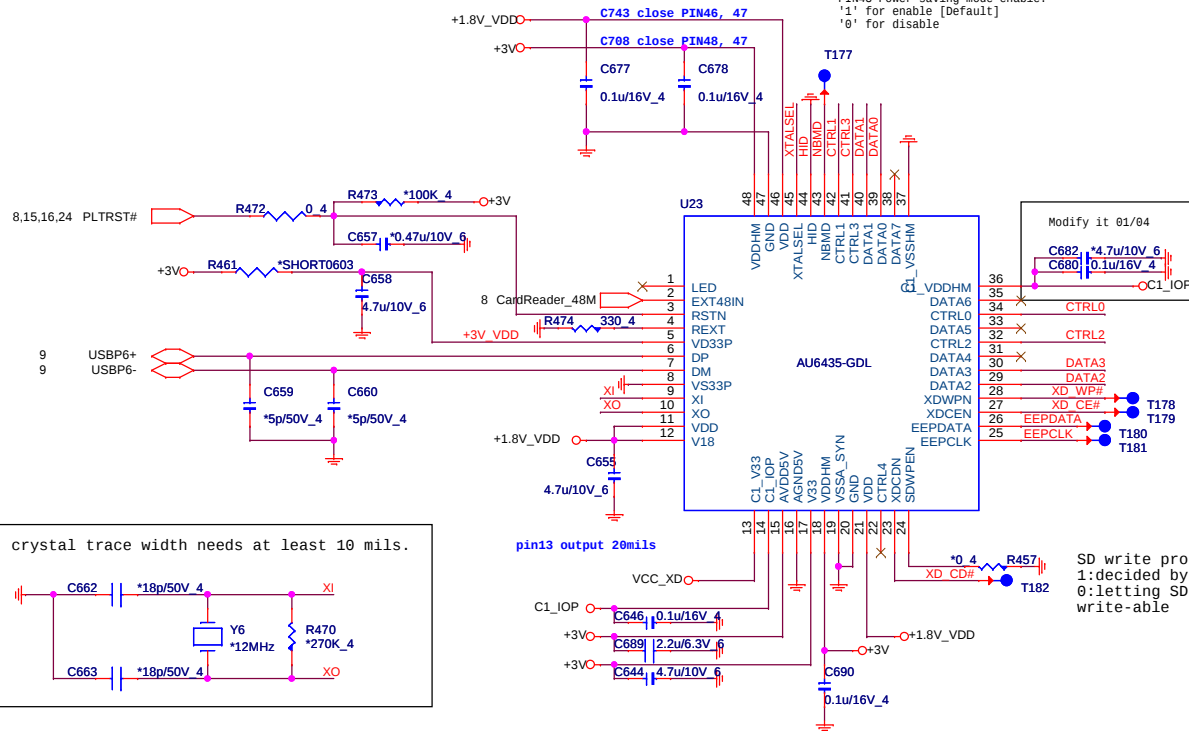


change R452 from CTRL1 to CTRL2
01/13

PIN45=Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input

R464 0.4 XTALSEL

PIN43=Power saving mode enable.
'1' for enable [Default]
'0' for disable



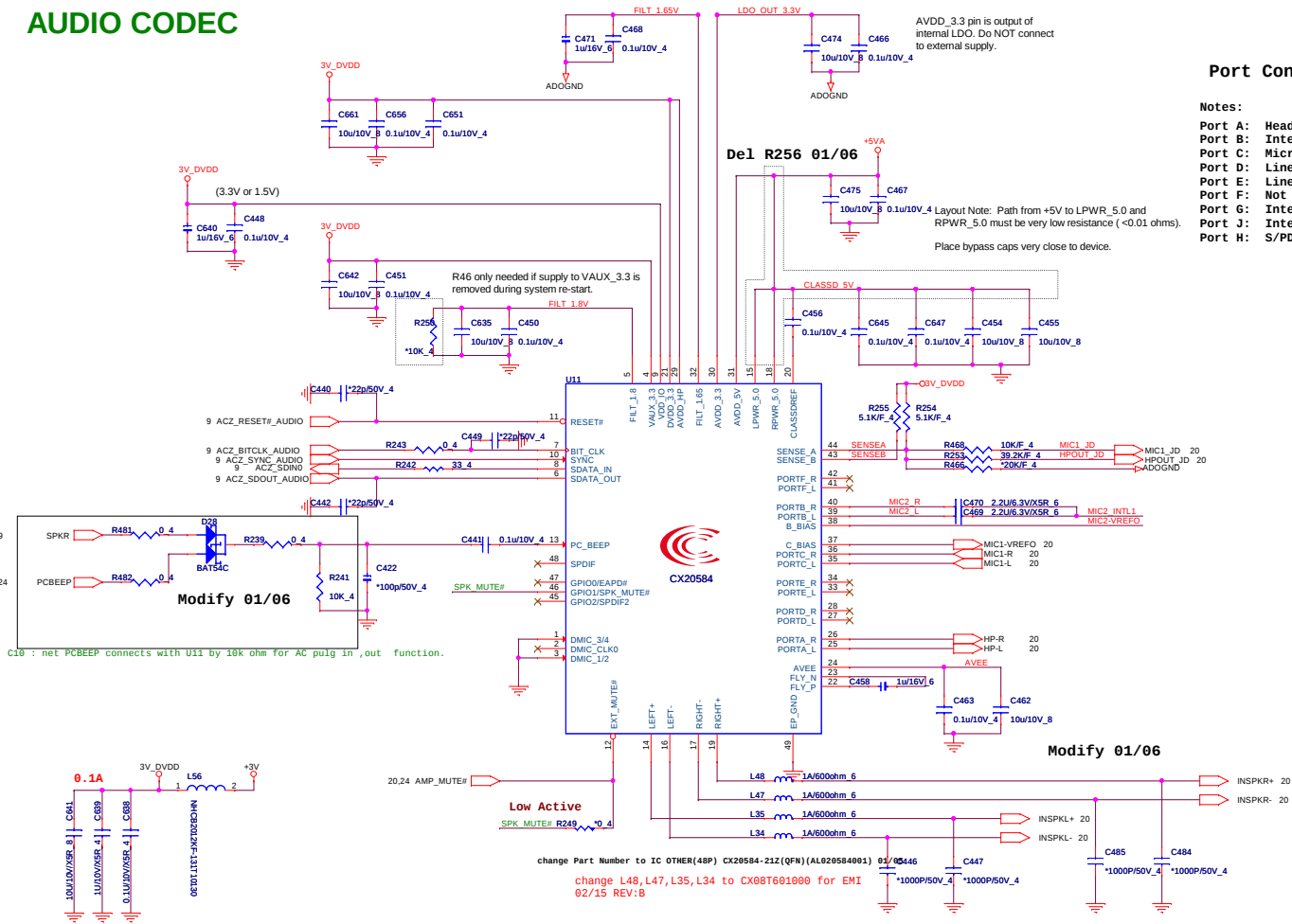
crystal trace width needs at least 10 mils.

SD write protect
1:decided by SDWP[Default]
0:letting SD always
write-able

Port Configuration

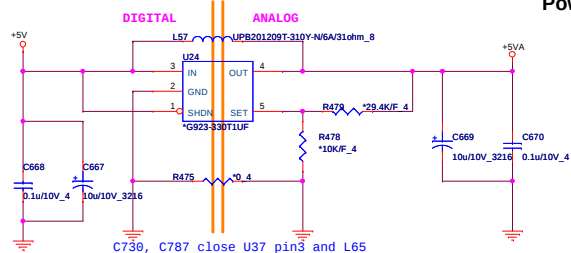
Notes:

- Port A: Headphone jack (jack shared with S/PDIF)
 Port B: Internal MIC (mono or stereo)
 Port C: Microphone/LI/L0 jack
 Port D: Line Out jack (Optional)
 Port E: Line In jack (Optional)
 Port F: Not used.
 Port G: Internal stereo speakers
 Port J: Internal stereo digital mic (Optional)
 Port H: S/PDIF (jack shared with headphone)

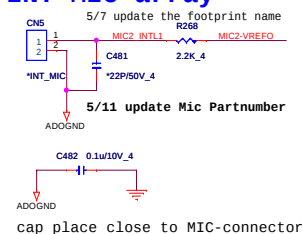


1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.
2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.
3. C309, C310, C311 are optional. Do not install unless needed for EMI/SI.

Power (ADO)



INT MIC array



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	CONEXANT 20584	1A
Date:	Translating March 15, 2011	Sheet 19 of 32

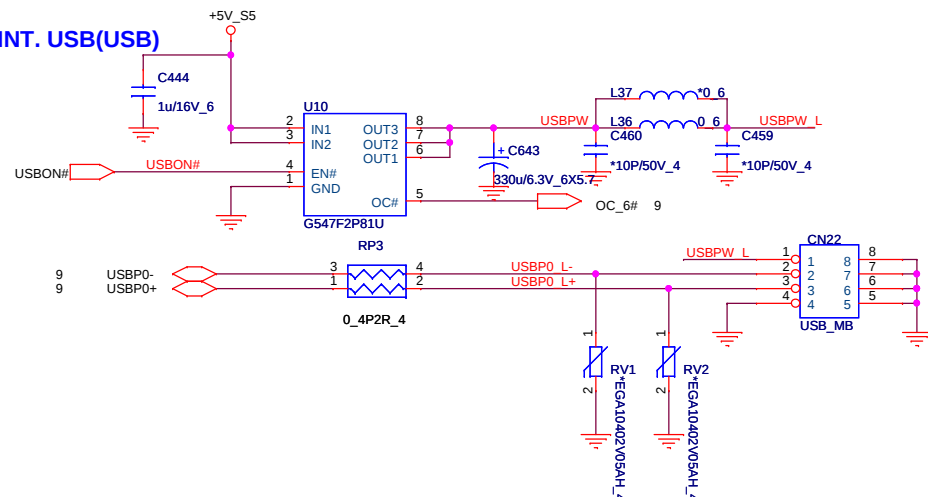
A



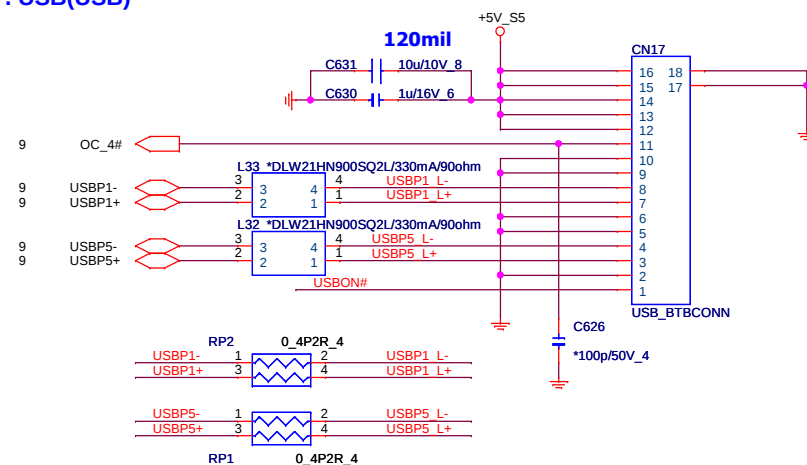
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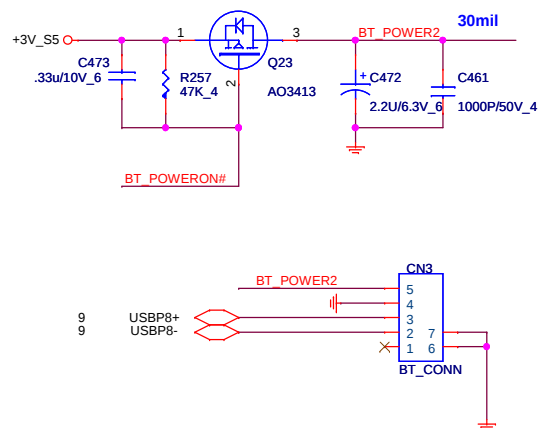
INT. USB(USB)



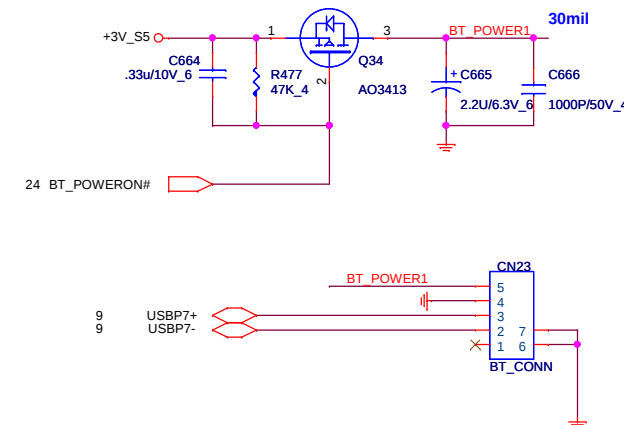
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



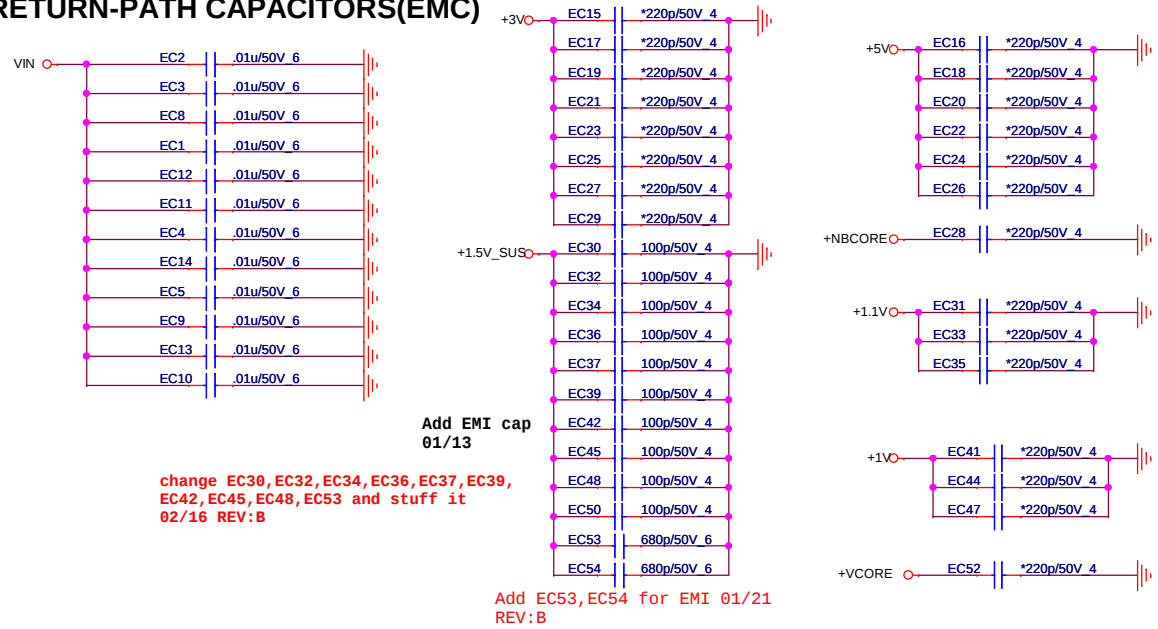
BLUETOOTH V3.0 CONN(BTM)



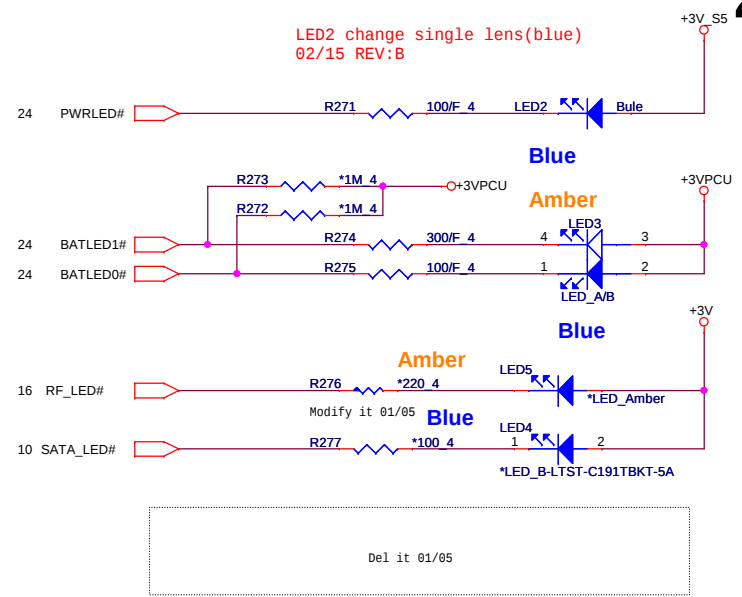
PROJECT : ZQP
Quanta Computer Inc.

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	USB/BT	1A
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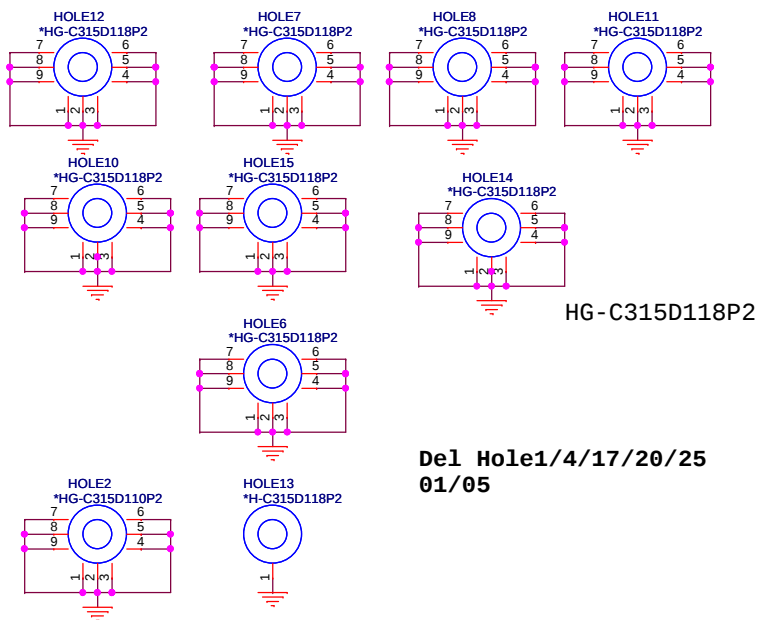
EE RETURN-PATH CAPACITORS(EMC)



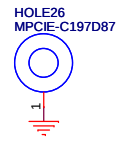
LED(UIF)



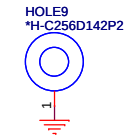
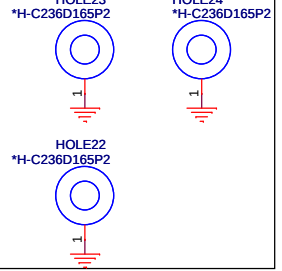
HOLE(OTH)



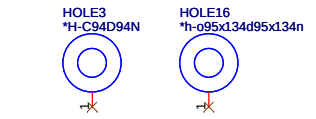
mini PCI



cpu



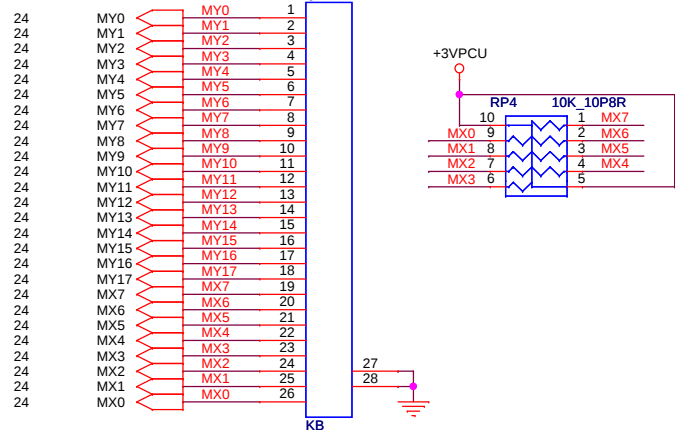
No stuff HOLE9 REV:B 02/17



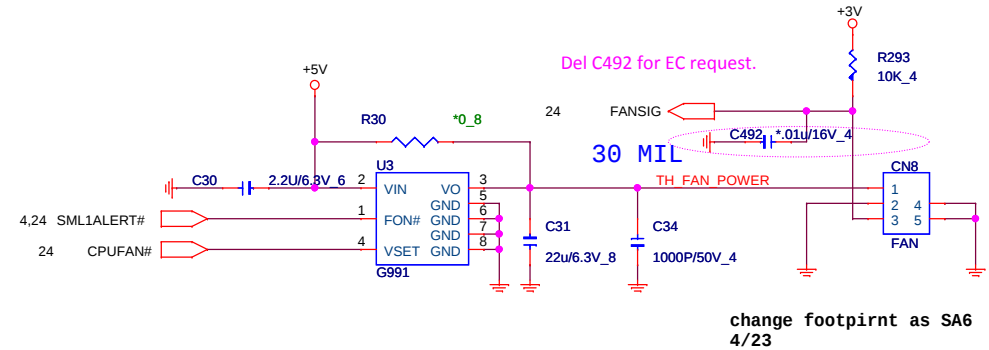
CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number	Rev
	LED/ EMI/ Screw Hole& Nut	1A
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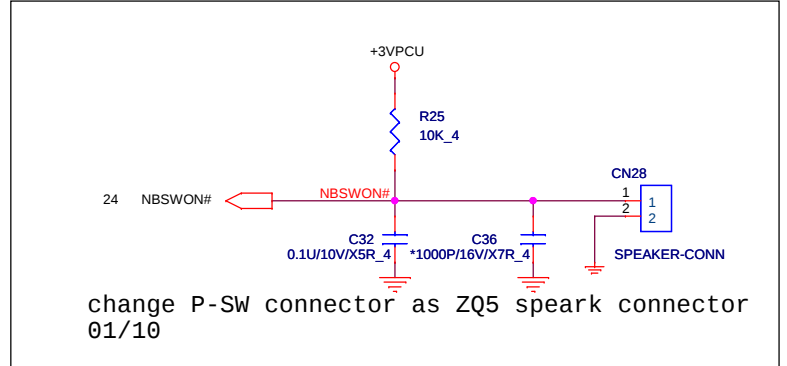
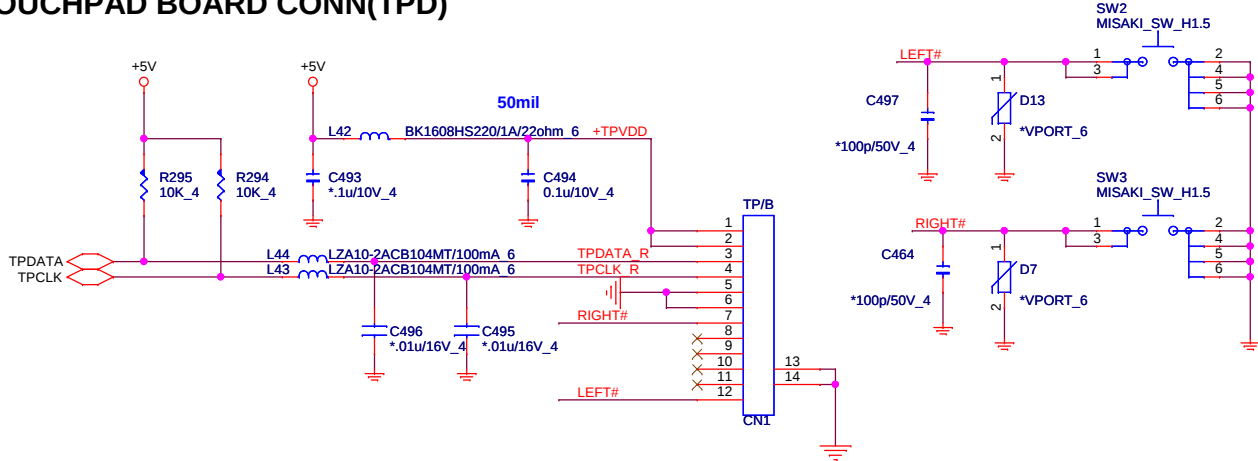
K/B(KBC)



CPU FAN(THM)

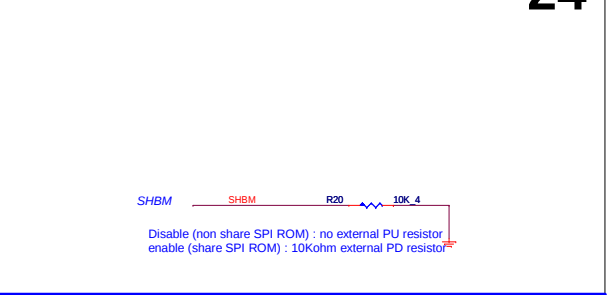
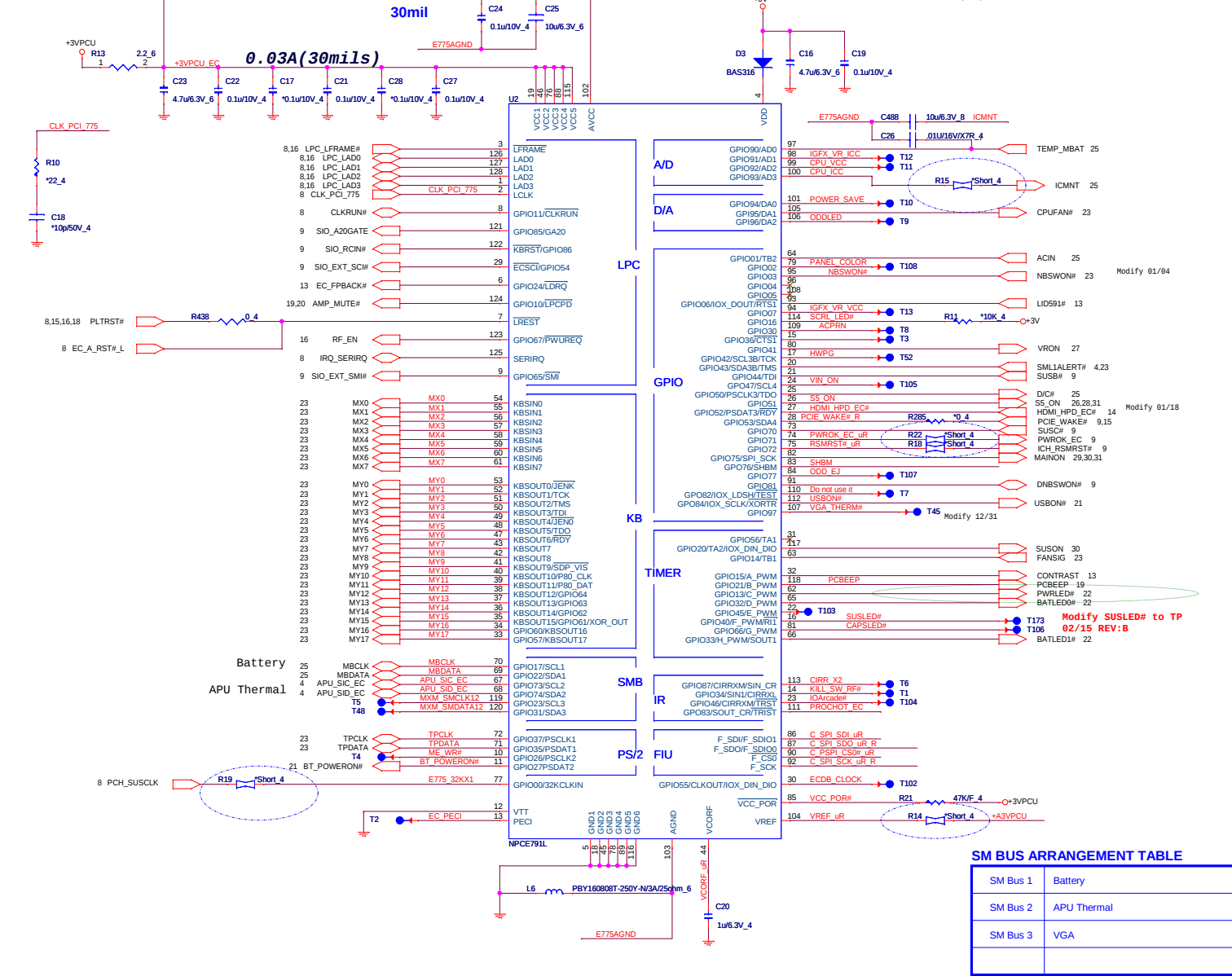


TOUCHPAD BOARD CONN(TPD)

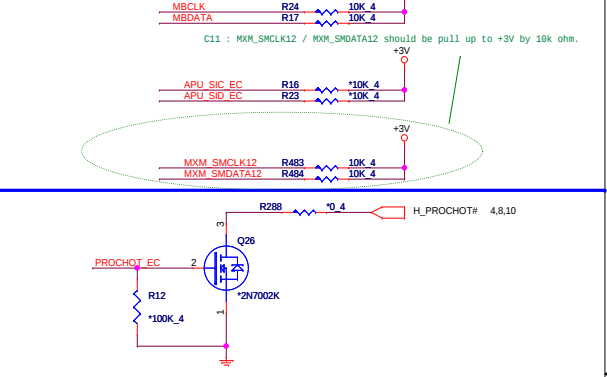


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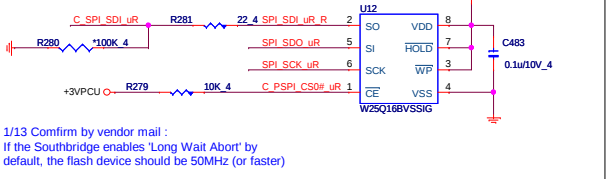
Size	Document Number	Rev
	KB/TP/FAN	1A
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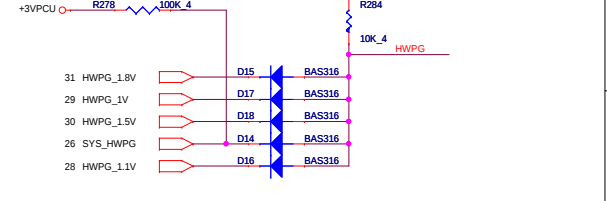
SM BUS PU(KBC)



SPI FLASH(KBC)



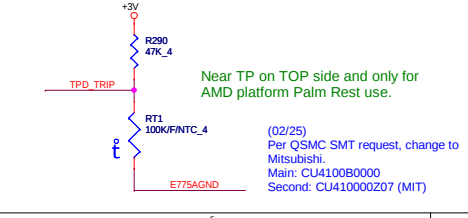
HWPG(KBC)



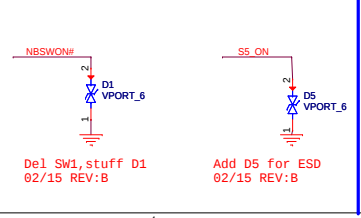
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

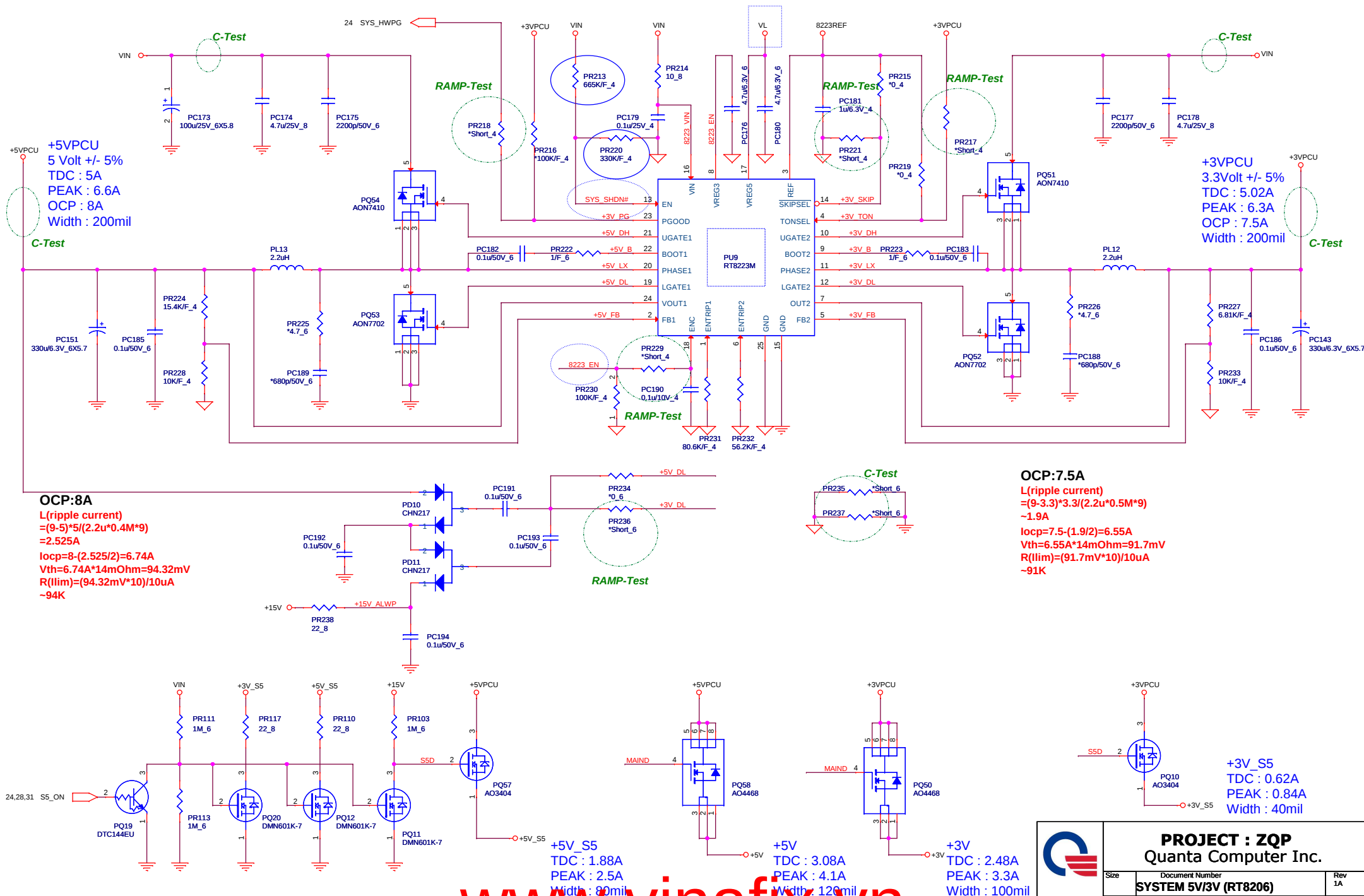
PALM REST THERMAL SENSOR (THM)

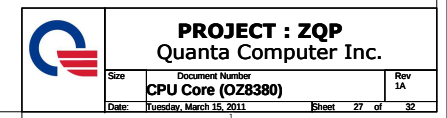


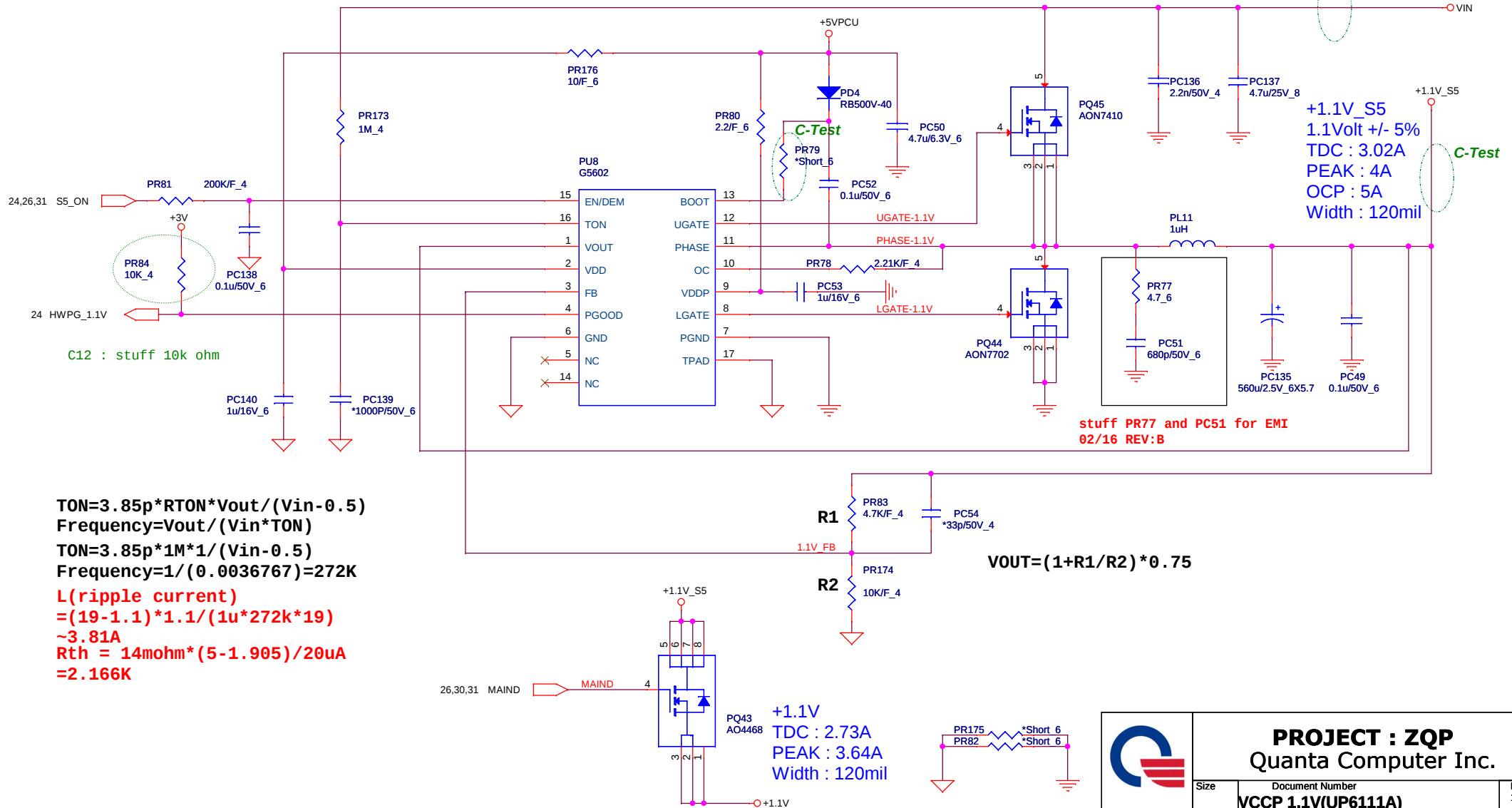
POWER-ON SWITCH (KBC)











$\text{TON} = 3.85\text{p} \cdot \text{RTON} \cdot \text{Vout} / (\text{Vin} - 0.5)$
 $\text{Frequency} = \text{Vout} / (\text{Vin} \cdot \text{TON})$
 $\text{TON} = 3.85\text{p} \cdot 1\text{M} \cdot 1 / (\text{Vin} - 0.5)$
 $\text{Frequency} = 1 / (0.0036767) = 272\text{K}$
L(ripple current)
 $= (19 - 1.1) \cdot 1.1 / (1\text{u} \cdot 272\text{k} \cdot 19)$
 $\sim 3.81\text{A}$
 $R_{\text{th}} = 14\text{mohm} \cdot (5 - 1.905) / 20\text{uA}$
 $= 2.166\text{K}$

+1.1V
TDC : 2.73A
PEAK : 3.64A
Width : 120mil



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change PR76 to 0 ohm for EMI
02/16 REV:B

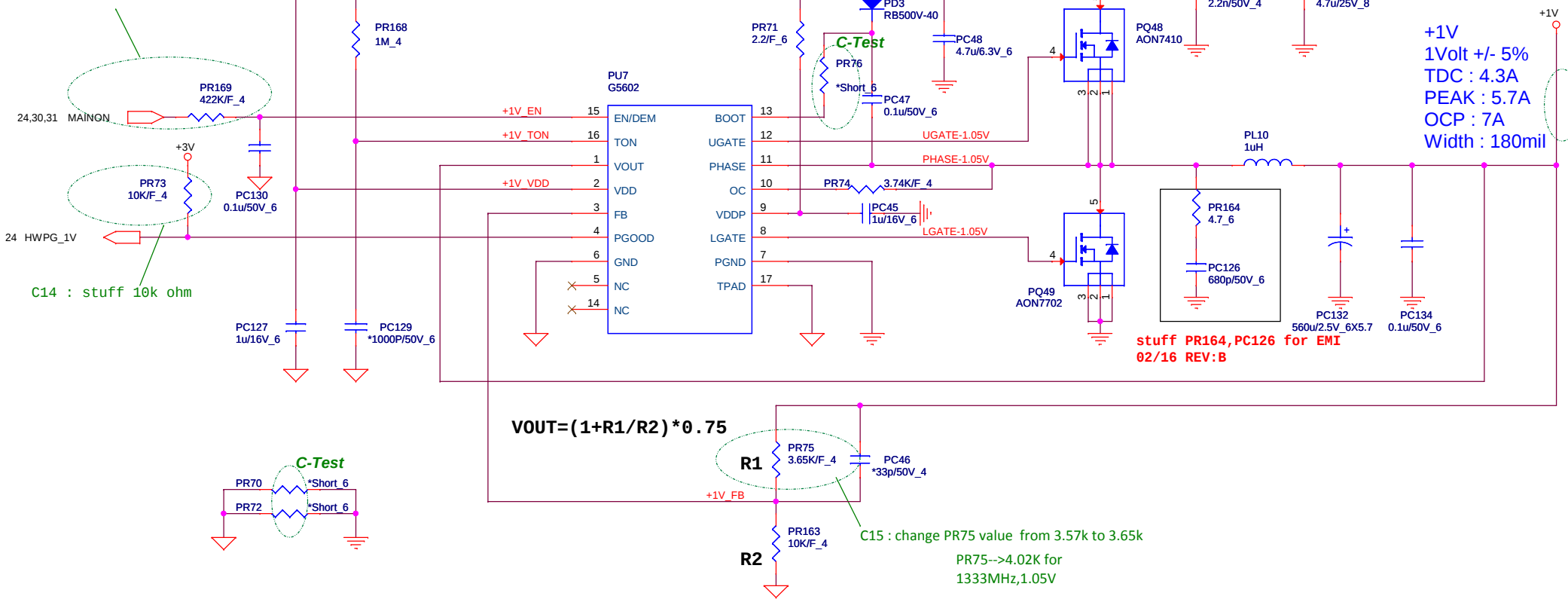
C-Test

+1V
1Volt +/- 5%
TDC : 4.3A
PEAK : 5.7A
OCP : 7A
Width : 180mil

C-Test

C13

change PR169 PN from 0ohm to 430kohm for timing issue

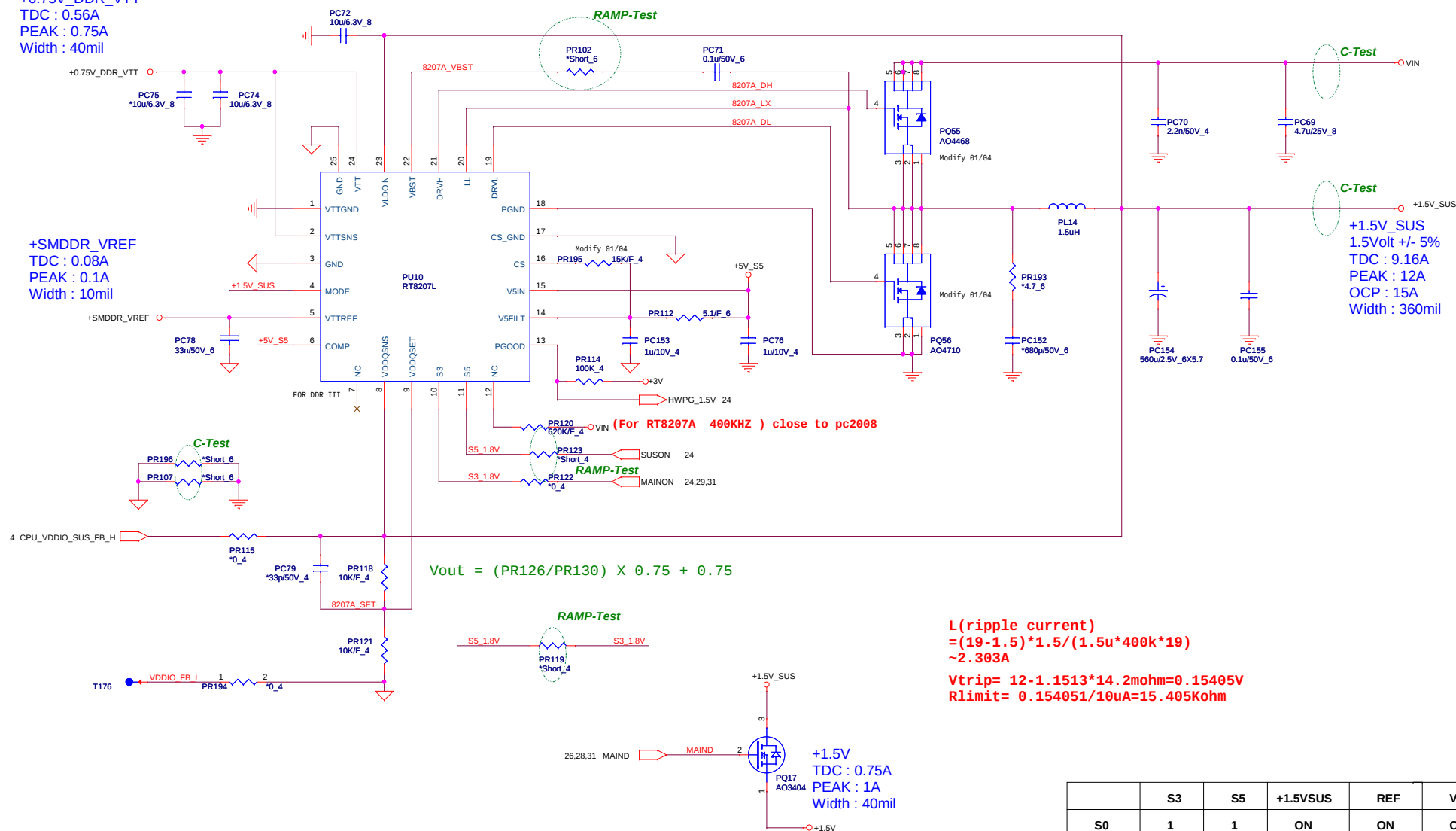


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Quanta Computer Inc.

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Date: Tuesday, March 15, 2011 Sheet 29 of 32

+0.75V_DDR_VTT
TDC : 0.56A
PEAK : 0.75A
Width : 40mil

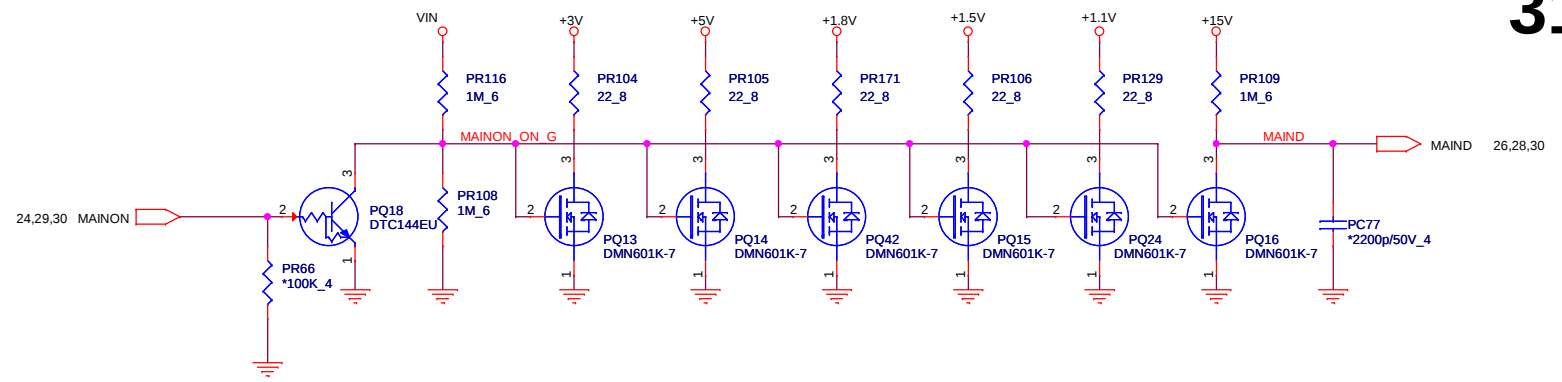


	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

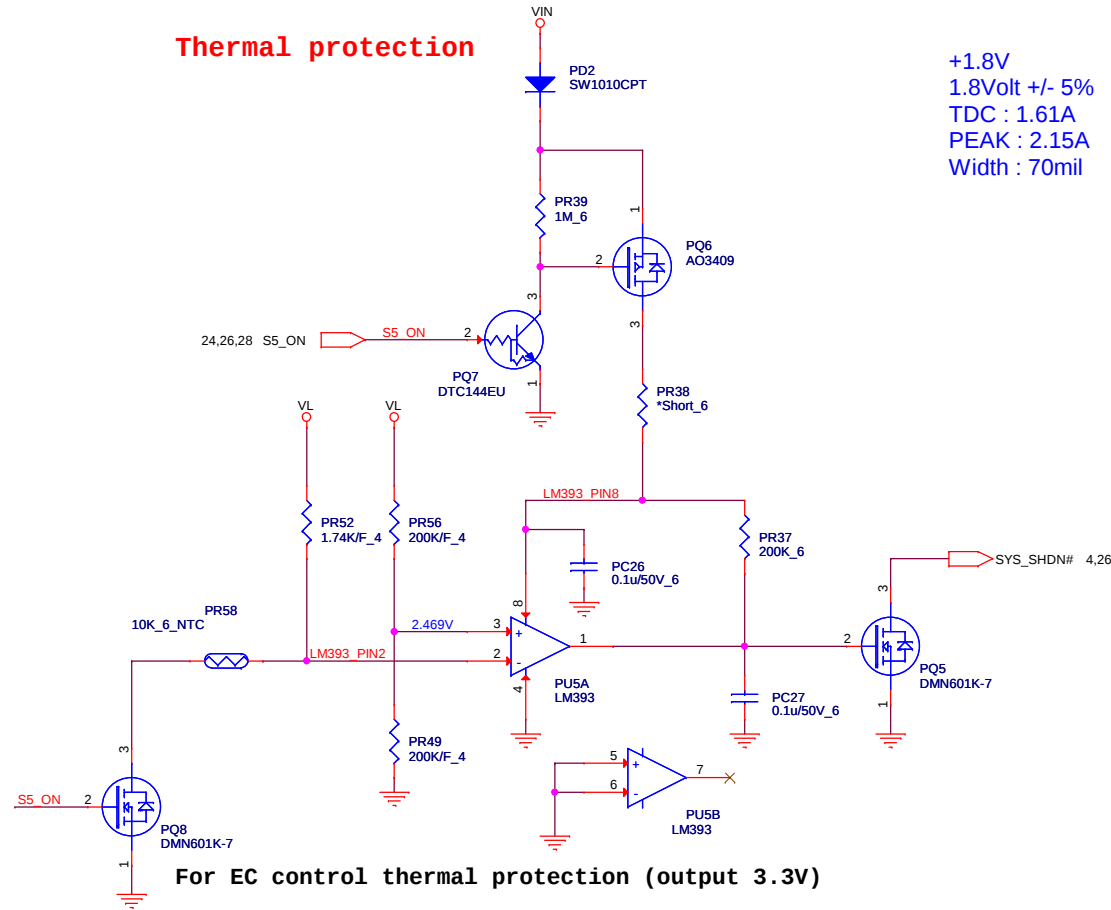


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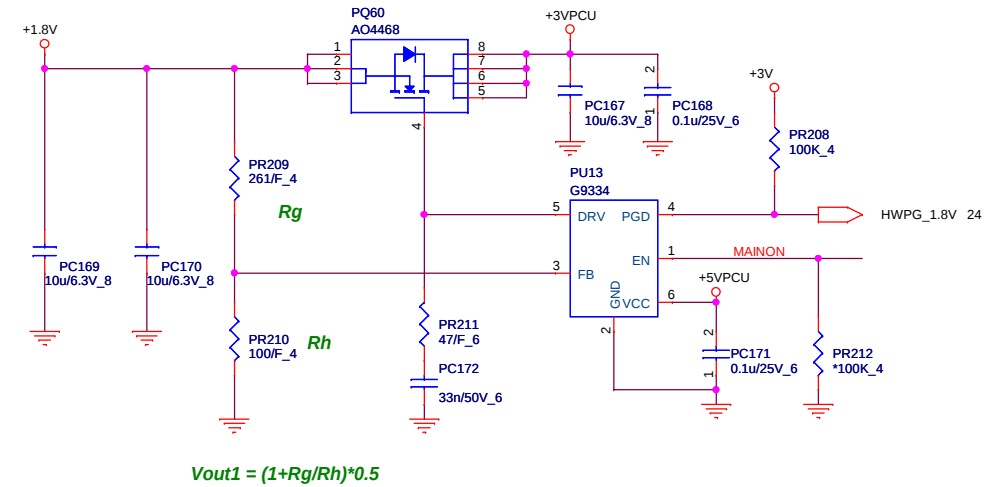
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Thermal protection



+1.8V
1.8V ± 5%
TDC : 1.61A
PEAK : 2.15A
Width : 70mil



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	Discharge /Thermal protection	1A
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MODEL	REV	CHANGE LIST	Model ZQE/G M/B BOARD		
			Page	From	To
ZQP/Q M/B	A	First Release	1	1A	3A
			2	1A	3A
			3	1A	3A
01.P14: Add HDMI function 02.P22: Add EC53,EC54 for EMI 03.P20: Stuff C673/C675/C671/C672 for EMI 04.P15: Stuff ESD protector at R31/R32 for EMI 05.P10: GPIO 58 define to HDMI strap pin 06.P08: Add C606,C614,C619 for strong clock 07.P20:change C673,C675,C671,C672 for EMI 08.P19:change L48,L47,L35,L34 to CX08T601000 for EMI 09.P24:No stuff SW1,stuff D1 10.P24:Add D5 on S5_ON for ESD 11.P22:LED2 change single lens(blue) 12.P08:Del C623 13.P24:Del SW1 14.P13:Del R26,R27 and add RP5 for EMI 15.P15:Add EC38,EC40,EC43,EC46 for EMI 16.P28:change PR79 to 0 ohm and stuff PR77 and PC51 for EMI 17.P29:change PR76 to 0 ohm and stuff PR164,PC126 for EMI 18.P27:stuff PR69,PC43 for EMI 19.P17:change C617,C612,C539,C540 footprint form 1206 to 0805 20.P13:Swap USB nets between L50 and PR5 21.P13:Add R33,R34 for ESD 22.P15:change C354 to CH122GK1I10 for EMI 23.P22:change EC30,EC32,EC34,EC36,EC37,EC39,EC42,EC45,EC48,EC53 and stuff it for EMI 24.P26:Remove JP20,JP21,JP22,JP23 and change to short pad PR235,PR237 25.P27:Remove JP10,JP9,JP6,JP8 and change to short pad PR55,PR48,PR43,PR46,PR47,PR54,PR63,PR142,PR140 26.P28:Remove JP24,JP25 27.P29:Remove JP16,JP17 and change to short pad PR70,PR72 28.P30:Remove JP18,JP19 and change to short pad PR196,PR107 29.P22:No stuff HOLE9	B		4	1A	3A
			5	1A	3A
			6	1A	3A
			7	1A	3A
			8	1A	3A
			9	1A	3A
			10	1A	3A
			11	1A	3A
			12	1A	3A
			13	1A	3A
			14	1A	3A
			15	1A	3A
			16	1A	3A
			17	1A	3A
			18	1A	3A
			19	1A	3A
			20	1A	3A
			21	1A	3A
			22	1A	3A
			23	1A	3A
			24	1A	3A
			25	1A	3A
			26	1A	3A
			27	1A	3A
			28	1A	3A
			29	1A	3A
			30	1A	3A
			31	1A	3A
			32	1A	3A
	33	1A	3A		
01.P15:change RJ45 connector without LED 02.P27:change PR140,PR142 to short pad 03.P30:change PR119,PR123,PR102 to short pad 04.P26:change PR217,PR218,PR221,PR229,PR236 to short pad 05.P29:change PR76 to short pad 06.P28:change PR79 to short pad	C		34	1A	3A
			35	1A	3A
			36	1A	3A
			37	1A	3A
			38	1A	3A
			39	1A	3A
			40	1A	3A
			41	1A	3A
Quanta Computer Inc. ZQP/Q		PROJECT : ZQP Quanta Computer Inc.		Size Document Number Rev	
				CHANGE LIST - 3A 1A	
PROJECT: ZQP/Q		PCBA NO.	REV: 3A	DOC. NO :	
APPROVED BY : Andy Lin		CHECK BY : Jia Huang	DRAWING BY : Andy Chen	DATE :10/18/2010	SHEET 1